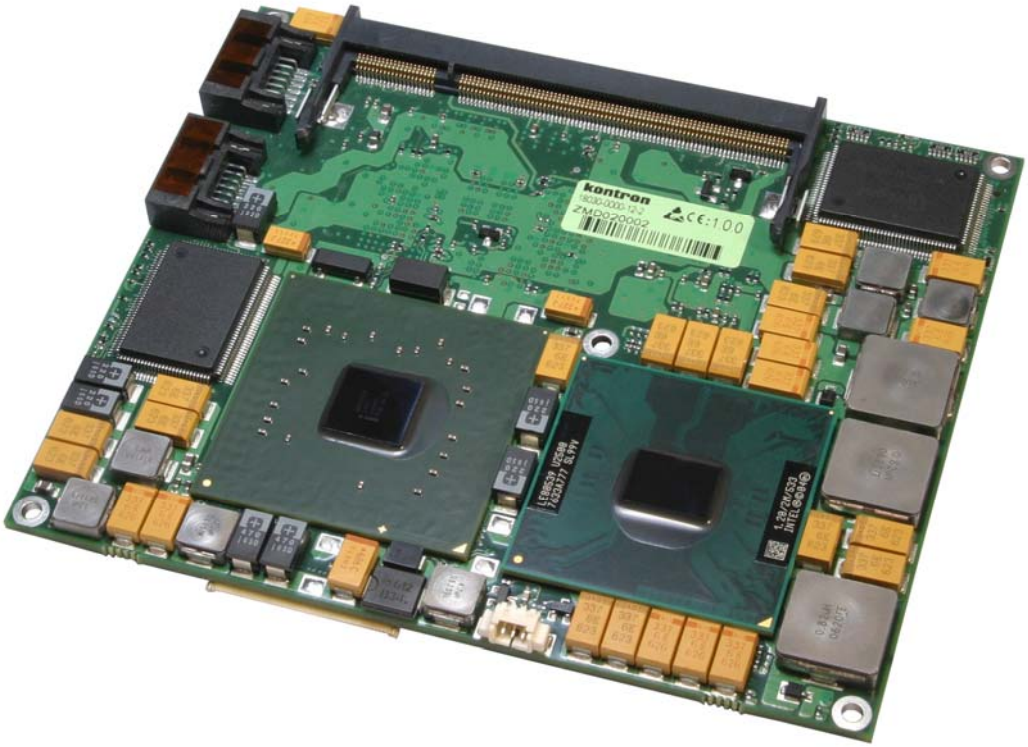
Kontron User's Guide



ETX® CD

Document Revision 1.0
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1 User Information

1.1 About This Document

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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

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Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 Introduction

2.1 ETX®-CD

Based on the ETX® standard, Kontron's ETX®-CD, powered by a variety of Intel Pentium core duo processors, is a next-generation embedded module that brings advanced technology to tomorrow's applications, as well as continuing today's legacy devices. Built around serial differential signaling technologies, ETX®-CD modules incorporate the following interfaces into a 95 x 114 small form factor embedded module:

- Core2Duo® (L7400) / Core Duo® (L2400 LV) / Core Solo® / Celeron® M (CM 423)
- PCI
- 2x Serial ATA (SATA)
- 1x Parallel ATA (IDE)
- USB
- 2x Serial Port (COM)
- 1x Parallel Port (LPT) shared with Floppy
- LVDS, SDVO, VGA
- 10/100 MB Ethernet
- ISA bus
- Audio
- Advanced Configuration and Power Interface (ACPI)

The ETX®-CD is built around the Intel Core Duo processors that use the Yonah and Merom Core and the Mobile Intel 945GME Express chipset, which is the first mobile platform to offer PCI Express functionality with extended life cycle support. These modules feature the most current desktop features such as USB, SATA, and PCI buses.

The ETX®-CD delivers up to 2GHz performance and up to 2GB DDR2 RAM. For applications that require advanced real-time video capabilities, the ETX®-CD has integrated graphics based on the Intel® Graphics Media Accelerator 900 architecture.

The ETX®-CD supports 4 PCI 32-bit PCI devices. A 10/100 megabits per second Ethernet port provides fast connectivity to LAN/WAN and 4x USB interface provides fast and sufficient interfaces for external peripherals.

ETX®-CD modules also provide the following interfaces that are always located in the same physical position on each board:

PCI32, USB, serial ATA (SATA), parallel ATA (PATA), LVDS Multi Media ports, as well as an ACPI (Advanced Configuration and Power Interface) for optimized power management are available on the board. Six mounting holes on the board provide secure mounting to allow the module increased shock and vibration resistance.

2.2 ETX® Documentation

This product manual serves as one of three principal references for an ETX® design. It documents the specifications and features of ETX®-CD. The other two references, which are available from the Kontron Embedded Modules Web site, include:

- The ETX® Specification defines the ETX® module form factor, pinout, and signals.
- The ETX® Design Guide serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of ETX® modules.

Note: Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.3 ETX® Benefits

Embedded technology extended (ETX) modules are very compact (114 x 95 mm), highly integrated computers. All ETX® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. This standardization allows designers to create a single-system baseboard that can accept present and future ETX® modules.

ETX® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- Parallel, Serial, and USB ports
- Keyboard/mouse
- Ethernet
- Sound
- IDE (and SATA)

The baseboard designer can optimize exactly how each of these functions implements physically.

Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

Peripheral PCI or ISA buses can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETX® modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a builtin upgrade path. The modularity of an ETX® solution also ensures against obsolescence as computer technology evolves. A properly designed ETX® baseboard can work with several successive generations of ETX® modules.

An ETX® baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specifications

3.1 Functional Specifications

Processor

The central processing unit (CPU) consists of:

Mobile Intel® Celeron® M, Intel® Core Solo®, Intel® Core Duo® or Intel® Core2Duo® processor (Codename Yonah/Merom) which includes such features as:

- First dual core processor for mobile
- Supports Intel® Architecture with Dynamic Execution
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache
- On-die, 2-MB second level cache with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3)
- The Intel Core Duo processor and Intel Core Solo processor in standard voltage and low voltage processors are offered at 667-MHz FSB
- Advanced power management features including Enhanced Intel SpeedStep® technology
- Digital thermal sensor (DTS)
- Execute Disable Bit support for enhanced security
- Intel® Virtualization Technology
- Deep C4 and Dynamic Cache Sizing

Bus

- 533 / 667 MHz CPU bus
- 400/533/667 MHz memory bus

Chipset:

- Intel® 945GM
- Intel® 82801GBM (ICH7-M)

Cache, Second level

- 1MB (Celeron® M)
- 2MB (Core Solo®)
- 2x1MB (Core Duo® and Core2Duo®)

System Memory

The ETX®-CD uses 200-pin DDR2 Small Outline-Dual Inline Memory Modules (SO-DIMMs). One socket is available for a DDR2-533 or DDR2-667 module up to 2GB capacity.

Note: ETX®-CD equipped with the CeleronM423 is not able to drive memory modules faster than DDR2-533.

Serial Digital Video Output (SDVO): Intel 945GM

- Concurrent Operation of PCI Express Graphics with SDVO
- Supports appropriate external SDVO components (DVI, LVDS, TV-out)

PCI 32: Intel ICH7

- Parallel PCI Bus 32 bit 33 MHz

Enhanced Intelligent Drive Electronics (EIDE): Intel ICH7

- One PCI Bus Master IDE port
- Supports 2 IDE devices
- Ultra 33 Direct Memory Access (DMA) mode
- Programmed Input/Output (PIO) modes up to Mode 4 timing
- Multiword DMA Mode 0,1,2 with independent timing

Serial ATA: Intel ICH7

- 2 Channels Serial ATA
- SATA Spec. Rev. 1.0 up to 150 MB/s per channel

Universal Serial Bus: Intel ICH7

- 4 USB
- USB legacy keyboard support
- USB floppy, CD-ROM, Hard drive, and memory stick boot support

10/100MB Ethernet:: Intel ICH7

- Fully compatible with IEEE 802.3

Onboard video graphics array (VGA): Intel® 945GM:

- Intel® Gen 3.5 Graphics engine
- Dynamic Video Memory Technology (DVMT 3.0)
- Cathode ray tube (CRT) up do QXGA
- low voltage differential signaling (LVDS) liquid-crystal display (LCD) and SDVO interfaces up to UXGA
- Supports DX 9.1

AC '97 (Audio): Intel 945GM;

- Up to 20 bit sample resolution
- Multiple sample rates up to 48bit
- Independent bus master logic for dual Microphone Input, dual PCM audio input, PCM audio input, modem input, modem output and S/PDIF output.

Trustes Platform Module (TPM)

- Can be equipped optionally
- Is currently not supported

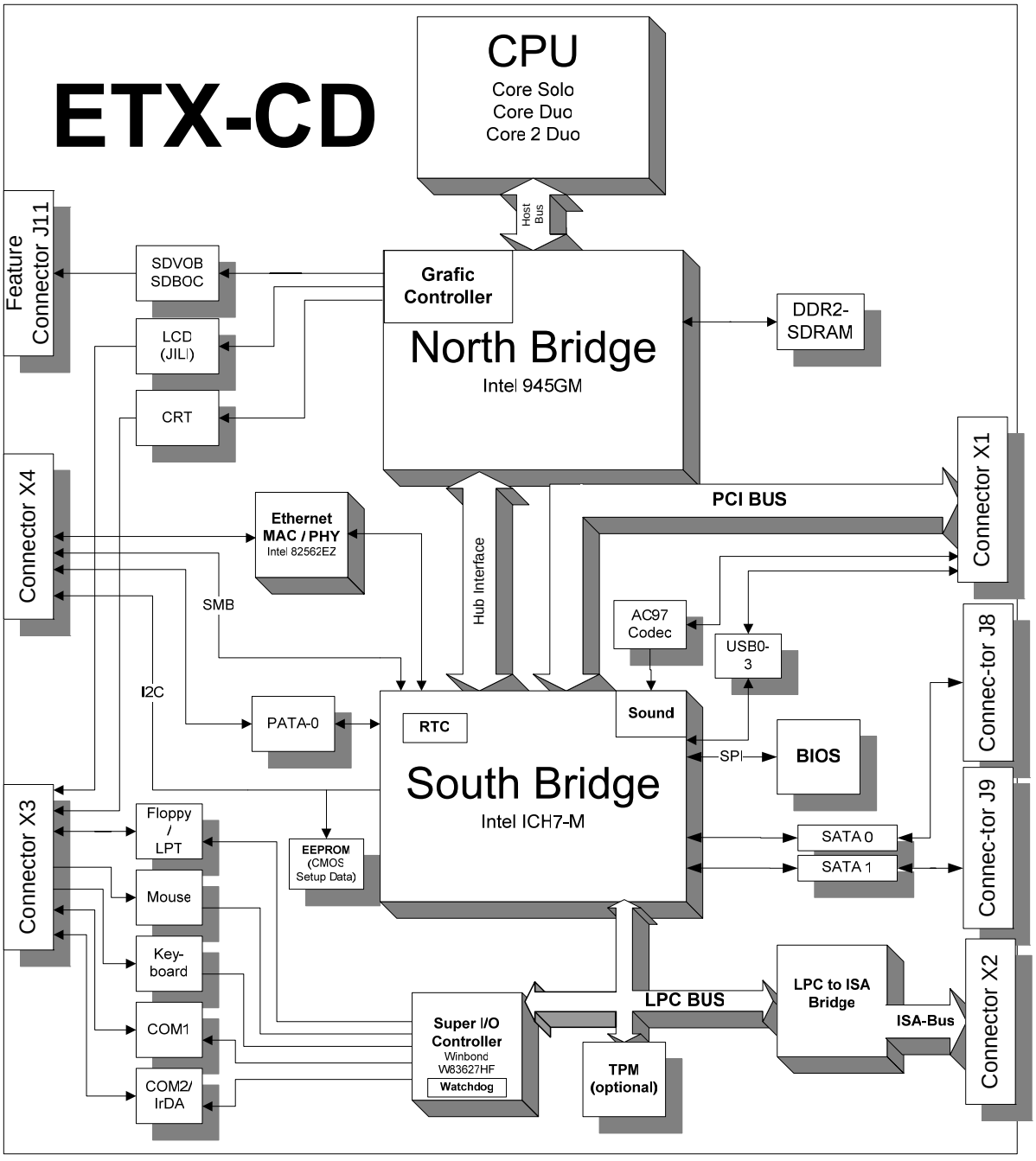
BIOS: Phoenix, 1MB Flash-BIOS in Firmware Hub Flash Memory

- NV-EEPROM for CMOS-setup retention without battery

Watchdog timer (WDT): Winbond Super I/O

Real-time clock (requires external battery)

3.1.1 Block diagram



3.2 Mechanical Specifications

3.2.1 Dimensions

- 95.0 mm x 114.0 mm
- Height approx. 12 mm (0.4")

Note: ***The maximum height of electrical components on the bottom side of the module is specified with 2.0mm in the ETX@ specification. On the ETX@-CD the Southbridge is soldered on the bottom side and Intel specified the ICH7 with 2.28mm ± 0.21mm***

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 5V DC +/- 5%

3.3.2 Supply Voltage Ripple

- Maximum 100 mV peak to peak 0 – 20 MHz

3.3.3 Supply Current 5 V_SB

- 0,10 A typical

3.3.4 Supply Current (typical, DOS prompt)

Power-consumption tests were executed during the DOS prompt and without a keyboard. Using a keyboard takes an additional 100 mA.

All tested boards were fully equipped –AL boards. All boards were equipped with 1024 MB DDR2 SDRAM.

Modules were tested using maximum CPU frequency.

ETX®-CD Celeron M ULV 423

CPU Clock	1066 MHz
Mode	Full On
Power Consumption	2,20 A

ETX®-CD Core 2 Duo Processor L7400

CPU Clock	2 x 1,5 GHz
Mode	Full On
Power Consumption	3,59 A

ETX®-CD Core Duo Processor L2400

CPU Clock	2 x 1,66 GHz
Mode	Full On
Power Consumption	2,96 A

ETX®-CD Core Duo Processor T2500

CPU Clock	2 x 2,0 GHz
Mode	Full On
Power Consumption	4,82 A

3.3.5 Power Consumption (Windows® XP SP2)

ETX® board	Full Load			Idle			Idle with C1E/EIST		
	[A]5V	[A]5VSB	[W]	[A]5V	[A]5VSB	[W]	[A]5V	[A]5VSB	[W]
T2500	6,70	tbd	**34,10**	3,35	tbd	**17,35**	1,92	tbd	**10,20**
L2400	4,22	tbd	**21,70**	2,25	tbd	**11,85**	1,85	tbd	**9,85**
L7400	6,51	0,41	**34,61**	2,74	0,02	**13,80**	2,67	0,02	**13,45**
CM423	2,51	tbd	**13,15**	1,87	tbd	**9,95**	np	np	**np**

ETX® board	Standby S1			Standby S3 cold			S3 hot		
	[A]5V	[A]5VSB	[W]	[A]5V	[A]5VSB	[W]	[A]5V	[A]5VSB	[W]
T2500	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
L2400	1,64	tbd	**8,80**	tbd	tbd	tbd	0,56	tbd	**3,40**
L7400	tbd	tbd	tbd	0,02	0,32	**1,67**	0,75	0,03	**3,91**
CM423	1,63	tbd	**8,75**	tbd	tbd	tbd	0,52	tbd	**3,20**

ETX® board	Soft Off (ACPI S5)	
	[A]5VSB	[W]
T2500	tbd	tbd
L2400	tbd	tbd
L7400	0,18	**0,90**
CM423	tbd	tbd

3.3.6 CMOS Battery Power Consumption

Voltage Range	Quiescent Current
2.0 V – 3.6 V	3,5 µA @ 2.5 V
	4,3 µA @ 3.0 V

CMOS battery power consumption was measured with an ETX®-CD module on a standard Kontron ETX® evaluation board. The system was turned off and the battery was removed from the evaluation board. The 2.5 V or 3.0 V of power was supplied from a DC power supply. Do not use these values to calculate the CMOS battery lifetime.

3.4 Environmental Specifications

3.4.1 Temperature

Operating: (with Kontron Embedded Modules heat-spreader plate assembly):

- Ambient temperature: 0°C to 60°C
- Maximum heatspreader-plate temperature: 0°C tp 60°C (*)

Non-operating:

- -30°C to 85°C

See the Thermal Management chapter for additional information.

*Note: *The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.*

Operating (without Kontron Embedded Modules heat-spreader plate assembly):

- Maximum operating temperature: 0°C to 60°C (**)

Non operating:

- -30° to +85°C

See the Thermal Management chapter for additional information.

*Note: **The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

3.5 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

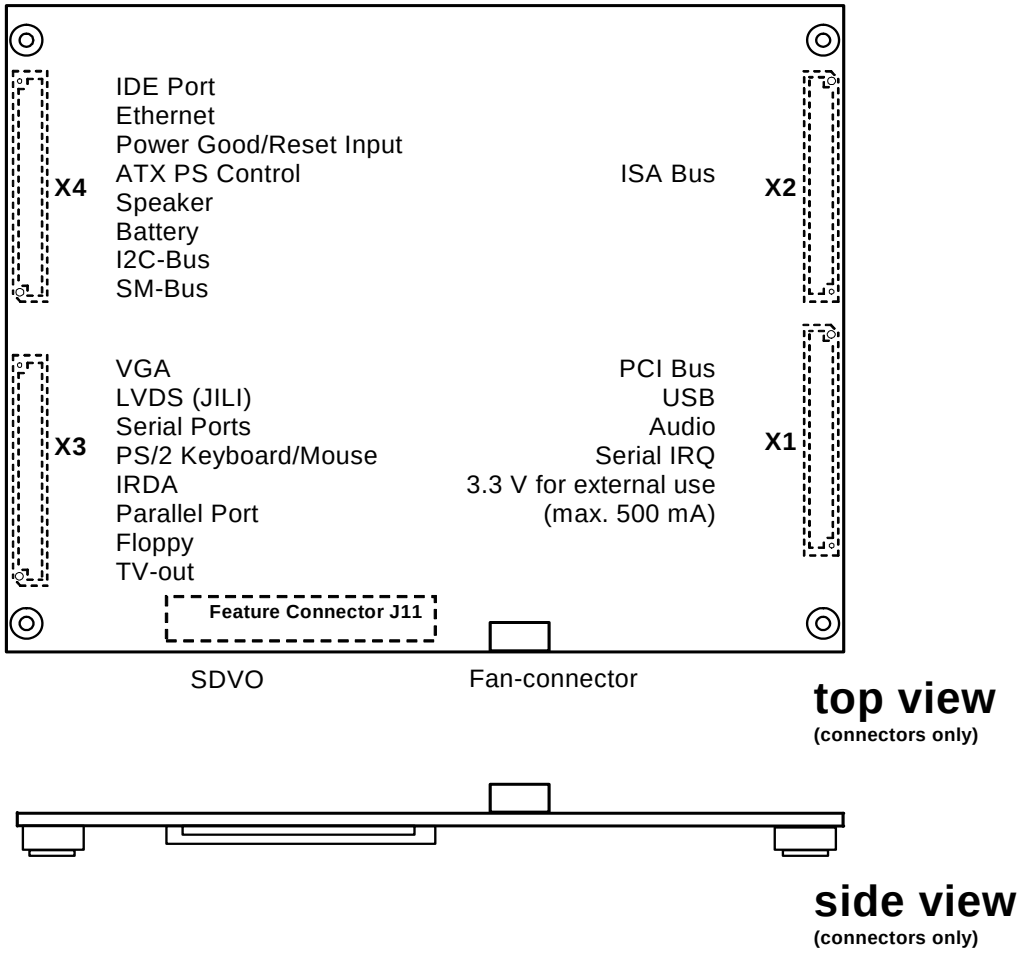
- System MTBF (hours) : 109418

Notes:	*Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement.* *Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.*

4 ETX® connectors

The pinouts for ETX® Interface Connectors X1, X2, X3, and X4 are documented for convenient reference. Please see the ETX® Specification and ETX® Design Guide for detailed, design-level information.

4.1 Connector Locations



4.2 General Signal Description

Term	Description
IO-3,3	Bi-directional 3,3 V IO-Signal
IO-5	Bi-directional 5 V IO-Signal
I-3,3	3,3 V Input
I-5	5 V Input
O-3,3	3,3 V Output
O-5	5 V Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection
Nc	Not Connected / Reserved

4.3 Connector X1 (PCI bus, USB, Audio)

Pin	Signal	Pin	Signal		Pin	Signal	Pin	Signal
1	GND	2	GND		51	VCC *	52	VCC *
3	PCICLK3	4	PCICLK4		53	PAR	54	SERR#
5	GND	6	GND		55	GPERR#	56	RESERVED
7	PCICLK1	8	PCICLK2		57	PME#	58	USB2#
9	REQ3#	10	GNT3#		59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V		61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#		63	IRDY#	64	STOP#
15	REQ1#	16	3V		65	FRAME#	66	USB2
17	GNT0#	18	RESERVED		67	GND	68	GND
19	VCC *	20	VCC *		69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#		71	AD17	72	USB3
23	AD0	24	3V		73	AD19	74	AD18
25	AD1	26	AD2		75	AD20	76	USB0#
27	AD4	28	AD3		77	AD22	78	AD21
29	AD6	30	AD5		79	AD23	80	USB1#
31	CBE0#	32	AD7		81	AD24	82	CBE3#
33	AD8	34	AD9		83	VCC *	84	VCC *
35	GND	36	GND		85	AD25	86	AD26
37	AD10	38	AUXAL		87	AD28	88	USB0
39	AD11	40	MIC		89	AD27	90	AD29
41	AD12	42	AUXAR		91	AD30	92	USB1
43	AD13	44	ASVCC		93	PCIRST#	94	AD31
45	AD14	46	SNDL		95	INTC#	96	INTD#
47	AD15	48	ASGND		97	INTA#	98	INTB#
49	CBE1#	50	SNDR		99	GND	100	GND

Notes: ** To protect external power lines of peripheral devices, make sure that:*
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.3.1 Connector X1 Signal Levels

Pin 1-50 [Power | PCI | USB | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	PCICLK3	PCI Clock Slot 3	O-3,3	-	-
4	PCICLK4	PCI Clock Slot 4	O-3,3	-	-
5	GND	Ground	PWR	-	-
6	GND	Ground	PWR	-	-
7	PCICLK1	PCI Clock Slot 1	O-3,3	-	-
8	PCICLK2	PCI Clock Slot 2	O-3,3	-	-
9	REQ3#	PCI Bus Request 3	I-3,3	PU 8k2 3.3V	8k2 Ohm Resistors
10	GNT3#	PCI Bus Grant 3	O-3,3	-	-
11	GNT2#	PCI Bus Grant 2	O-3,3	-	-
12	3V	Power +3,3V	PWR	-	-
13	REQ2#	PCI Bus Request 2	I-3,3	PU 8k2 3.3V	8k2 Ohm Resistors
14	GNT1#	PCI Bus Grant 1	O-3,3	-	-
15	REQ1#	PCI Bus Request 1	I-3,3	PU 8k2 3.3V	8k2 Ohm Resistors
16	3V	Power +3,3V	PWR	-	-
17	GNT0#	PCI Bus Grant 0	O-3,3	-	-
18	nc	-	nc	-	Reserved
19	VCC	Power +5V	PWR	-	-
20	VCC	Power +5V	PWR	-	-
21	SERIRQ	Serial Interrupt Reqest	IO-3,3	-	12mA Source sink
22	REQ0#	PCI Bus Request 0	I-3,3	PU 8k2 3.3V	8k2 Ohm Resistors
23	AD0	PCI Adress & Data Bus line	IO-3,3		-
24	3V	Power +3,3V	PWR	-	-
25	AD1	PCI Adress & Data Bus line	IO-3,3	-	-
26	AD2	PCI Adress & Data Bus line	IO-3,3	-	-
27	AD4	PCI Adress & Data Bus line	IO-3,3	-	-
28	AD3	PCI Adress & Data Bus line	IO-3,3	-	-
29	AD6	PCI Adress & Data Bus line	IO-3,3	-	-
30	AD5	PCI Adress & Data Bus line	IO-3,3	-	-
31	CBE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
32	AD7	PCI Adress & Data Bus line	IO-3,3	-	-
33	AD8	PCI Adress & Data Bus line	IO-3,3	-	-
34	AD9	PCI Adress & Data Bus line	IO-3,3	-	-
35	GND	Ground	PWR	-	-
36	GND	Ground	PWR	-	-
37	AD10	PCI Adress & Data Bus line	IO-3,3	-	-
38	AUXAL	Auxiliary Line Input Left	I	PD 4k7 ASGND	1:2 bleeder
39	AD11	PCI Adress & Data Bus line	IO-3,3	-	-
40	MIC	Microphone Input	I	-	-
41	AD12	PCI Adress & Data Bus line	IO-3,3	-	-
42	AUXAR	Auxiliary Line Input Right	I	PD 4k7 ASGND	1:2 bleeder
43	AD13	PCI Adress & Data Bus line	IO-3,3	-	-
44	ASVCC	Analog Supply of Sound Controller	O-5	-	-
45	AD14	PCI Adress & Data Bus line	IO-3,3	-	-
46	SNDL	Audio Out Left	O	-	-
47	AD15	PCI Adress & Data Bus line	IO-3,3	-	-
48	ASGND	Analog Ground of Sound Controller	P	-	-
49	CBE1#	PCI Bus Command and Byte enables 1	IO-3,3	-	-
50	SNDR	Audio Out Right	O	-	-

Note: The termination resistors in this table are already mounted on the ETX®board. Please refer to the design guide for information about additional termination resistors.

Pin 51–100: [Power | PCI | USB | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
51	VCC	Power +5V	PWR	-	-
52	VCC	Power +5V	PWR	-	-
53	PAR	PCI Bus Parity	IO-3,3	-	-
54	SERR#	PCI Bus System Error	IO-3,3	PU 8k2 3,3V	-
55	GPERR#	PCI Bus Grant Error	IO-3,3	PU 8k2 3,3V	-
56	nc	-	nc	-	Reserved
57	PME#	PCI Power Management Event	IO-3,3	-	int. PU 20k 3,3V
58	USB2#	USB Data- , Port2	IO-3,3	-	int. PD 15k in ICH7
59	LOCK#	PCI Bus Lock	IO-3,3	PU 8k2 3,3V	-
60	DEVSEL#	PCI Bus Device Select	IO-3,3	PU 8k2 3,3V	-
61	TRDY#	PCI Bus Target Ready	IO-3,3	PU 8k2 3,3V	-
62	USB3#	USB Data- , Port3	IO-3,3	-	int. PD 15k in ICH7
63	IRDY#	PCI Bus Initiator Ready	IO-3,3	PU 8k2 3,3V	-
64	STOP#	PCI Bus Stop	IO-3,3	PU 8k2 3,3V	-
65	FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 8k2 3,3V	-
66	USB2	USB Data+ , Port2	IO-3,3	-	int. PD 15k in ICH7
67	GND	Ground	PWR	-	-
68	GND	Ground	PWR	-	-
69	AD16	PCI Adress & Data Bus line	IO-3,3	-	-
70	CBE2#	PCI Bus Command and Byte enables 2	IO-3,3	-	-
71	AD17	PCI Adress & Data Bus line	IO-3,3	-	-
72	USB3	USB Data+ , Port3	IO-3,3	-	int. PD 15k in ICH7
73	AD19	PCI Adress & Data Bus line	IO-3,3	-	-
74	AD18	PCI Adress & Data Bus line	IO-3,3	-	-
75	AD20	PCI Adress & Data Bus line	IO-3,3	-	-
76	USB0#	USB Data- , Port0	IO-3,3	-	int. PD 15k in ICH7
77	AD22	PCI Adress & Data Bus line	IO-3,3	-	-
78	AD21	PCI Adress & Data Bus line	IO-3,3	-	-
79	AD23	PCI Adress & Data Bus line	IO-3,3	-	-
80	USB1#	USB Data- , Port1	IO-3,3	-	int. PD 15k in ICH7
81	AD24	PCI Adress & Data Bus line	IO-3,3	-	-
82	CBE3#	PCI Command and Byte enables 3	IO-3,3	-	-
83	VCC	Power +5V	PWR	-	-
84	VCC	Power +5V	PWR	-	-
85	AD25	PCI Adress & Data Bus line	IO-3,3	-	-
86	AD26	PCI Adress & Data Bus line	IO-3,3	-	-
87	AD28	PCI Adress & Data Bus line	IO-3,3	-	-
88	USB0	USB Data+ , Port0	IO-3,3	-	int. PD 15k in ICH7
89	AD27	PCI Adress & Data Bus line	IO-3,3	-	-
90	AD29	PCI Adress & Data Bus line	IO-3,3	-	-
91	AD30	PCI Adress & Data Bus line	IO-3,3	-	-
92	USB1	USB Data+ , Port1	IO-3,3	-	int. PD 15k in ICH7
93	PCIRST#	PCI Bus Reset	O-3,3	-	-
94	AD31	PCI Adress & Data Bus line	IO-3,3	-	-
95	INTC#	PCI BUS Interrupt Request C	I-3,3	PU 8k2 3,3V	-
96	INTD#	PCI BUS Interrupt Request D	I-3,3	PU 8k2 3,3V	-
97	INTA#	PCI BUS Interrupt Request A	I-3,3	PU 8k2 3,3V	-
98	INTB#	PCI BUS Interrupt Request B	I-3,3	PU 8k2 3,3V	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

4.3.2 Connector X1 Signal Description

PCI Bus

The implementation of this subsystem complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

USB

Three USB host controllers (two 1.1 UHCI and one EHCI high-speed 2.0 controller) are on the Intel® 82801GB south bridge device. The USB controllers comply with both versions 1.1 and 2.0 of the USB standard and are backward compatible. The three controllers implement a root hub, which have two USB ports each.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

Audio

The ETX®-CD PCI audio controller is integrated in the Intel® 82801GB southbridge. The audio codec is compatible with AC97.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Continuous Mode” per default and can be changed in the BIOS setup, the frame size is 21 frames and the start frame pulse width is 4 clocks.

3.3V Power Supply for External Components

The ETX®-CD offers the ability to connect external 3.3V devices to the onboard-generated supply voltage. Pin 12 and Pin 16 of Connector X1 are used to connect to the +3.3V ±5% power supply. The maximum external load is 500mA. Contact Kontron Embedded Systems Technical Support for help with this feature.

Warning: Do not connect 3.3 V pins to external 3.3 V supply.

For additional information, refer to the ETX® Design Guide, I2C application notes, and JIDA specifications, all of which are available on the Kontron Embedded Systems Web site.

4.4 Connector X2 (ISA Bus)

Pin	Signal	Pin	Signal		Pin	Signal	Pin	Signal
1	GND	2	GND		51	VCC *	52	VCC *
3	SD14	4	SD15		53	SA6	54	IRQ5
5	SD13	6	MASTER#		55	SA7	56	IRQ6
7	SD12	8	DREQ7		57	SA8	58	IRQ7
9	SD11	10	DACK7#		59	SA9	60	SYSCLK
11	SD10	12	DREQ6		61	SA10	62	REFSH#
13	SD9	14	DACK6#		63	SA11	64	DREQ1
15	SD8	16	DREQ5		65	SA12	66	DACK1#
17	MEMW#	18	DACK5#		67	GND	68	GND
19	MEMR#	20	DREQ0		69	SA13	70	DREQ3
21	LA17	22	DACK0#		71	SA14	72	DACK3#
23	LA18	24	IRQ14		73	SA15	74	IOR#
25	LA19	26	IRQ15		75	SA16	76	IOW#
27	LA20	28	IRQ12		77	SA18	78	SA17
29	LA21	30	IRQ11		79	SA19	80	SMEMR#
31	LA22	32	IRQ10		81	IOCHRDY	82	AEN
33	LA23	34	IO16#		83	VCC *	84	VCC *
35	GND	36	GND		85	SD0	86	SMEMW#
37	SBHE#	38	M16#		87	SD2	88	SD1
39	SA0	40	OSC		89	SD3	90	NOWS#
41	SA1	42	BALE		91	DREQ2	92	SD4
43	SA2	44	TC		93	SD5	94	IRQ9**
45	SA3	46	DACK2#		95	SD6	96	SD7
47	SA4	48	IRQ3		97	IOCHK#	98	RSTDRV
49	SA5	50	IRQ4		99	GND	100	GND

Notes: **To protect external power lines of peripheral devices, make sure that:*
- The wires have the right diameter to withstand the maximum available current.
- The enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950
*** IRQ9 is used for SCI in ACPI mode. Do not use for legacy ISA devices.*

4.4.1 Connector X2 Signal Levels

Pin 1–50: [Power | ISA]

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	SD14	ISA Data Bus	IO-5	PU 8k2 5V	-
4	SD15	ISA Data Bus	IO-5	PU 8k2 5V	-
5	SD13	ISA Data Bus	IO-5	PU 8k2 5V	-
6	MASTER#	ISA 16-Bit Master	I-5	PU 330R 5V	-
7	SD12	ISA Data Bus	IO-5	PU 8k2 5V	-
8	DREQ7	ISA DMA Request 7	I-5	PU 8k2 5V	-
9	SD11	ISA Data Bus	IO-5	PU 8k2 5V	-
10	DACK7#	ISA DMA Acknowledge 7	IO-5	-	24mA source cap.
11	SD10	ISA Data Bus	IO-5	PU 8k2 5V	-
12	DREQ6	ISA DMA Request 6	I-5	PU 8k2 5V	-
13	SD9	ISA Data Bus	IO-5	PU 8k2 5V	-
14	DACK6#	ISA DMA Acknowledge 6	IO-5	-	24mA source cap.
15	SD8	ISA Data Bus	IO-5	PU 8k2 5V	-
16	DREQ5	ISA DMA Request 5	I-5	PU 8k2 5V	-
17	MEMW#	ISA Memory Write	IO-5	PU 8k2 5V	-
18	DACK5#	ISA DMA Acknowledge 5	IO-5	-	24mA source cap.
19	MEMR#	ISA Memory Read	IO-5	PU 8k2 5V	-
20	DREQ0	ISA DMA Request 0	I-5	PU 8k2 5V	-
21	LA17	ISA Adress Bus (SA17)	O-5	-	-
22	DACK0#	ISA DMA Acknowledge 0	IO-5	-	24mA source cap.
23	LA18	ISA Adress Bus (SA18)	O-5	-	-
24	IRQ14	ISA Interrupt Request 14 / ROM Chip Select	IO-5	PU 8k2 5V	-
25	LA19	ISA Adress Bus (SA19)	O-5	-	-
26	IRQ15	ISA Interrupt Request 15	I-5	PU 8k2 5V	-
27	LA20	ISA Latchable Adress Bus	O-5	-	-
28	IRQ12	ISA Interrupt Request 12	I-5	PU 8k2 5V	-
29	LA21	ISA Latchable Adress Bus	O-5	-	-
30	IRQ11	ISA Interrupt Request 11	I-5	PU 8k2 5V	-
31	LA22	ISA Latchable Adress Bus	O-5	-	-
32	IRQ10	ISA Interrupt Request 10	I-5	PU 8k2 5V	-
33	LA23	ISA Latchable Adress Bus	O-5	-	-
34	IO16#	ISA 16-Bit I/O Access	I-5	PU 330R 5V	-
35	GND	Ground	PWR	-	-
36	GND	Ground	PWR	-	-
37	SBHE#	ISA System Byte High Enable	IO-5	-	-
38	M16#	ISA 16-Bit Memory Access	IO-5	PU 330R 5V	-
39	SA0	ISA Adress Bus	O-5	PU 8k2 5V	-
40	OSC	ISA Oscillator (CLK_ISA14#)	O-3,3	-	-
41	SA1	ISA Adress Bus	O-5	PU 8k2 5V	-
42	BALE	ISA Buffer Adress Latch Enable	IO-5	-	-
43	SA2	ISA Adress Bus	O-5	PU 8k2 5V	-
44	TC	ISA Terminal Count	IO-5	-	-
45	SA3	ISA Adress Bus	O-5	PU 8k2 5V	-
46	DACK2#	ISA DMA Acknowledge 2	IO-5	-	-
47	SA4	ISA Adress Bus	O-5	PU 8k2 5V	-
48	IRQ3	ISA Interrupt Request 3	I-5	PU 8k2 5V	-
49	SA5	ISA Adress Bus	O-5	PU 8k2 5V	-
50	IRQ4	ISA Interrupt Request 4	I-5	PU 8k2 5V	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

Pin 51-100: [Power | ISA]

Pin	Signal	Description	Type	Termination	Comment
51	VCC	Power +5V	PWR	-	-
52	VCC	Power +5V	PWR	-	-
53	SA6	ISA Adress Bus	O-3,3	PU 8k2 5V	-
54	IRQ5	ISA Interrupt Request 5	I-3,3	PU 8k2 5V	-
55	SA7	ISA Adress Bus	O-3,3	PU 8k2 5V	-
56	IRQ6	ISA Interrupt Request 6	I-3,3	PU 8k2 5V	-
57	SA8	ISA Adress Bus	O-3,3	PU 8k2 5V	-
58	IRQ7	ISA Interrupt Request 7	I-3,3	PU 8k2 5V	-
59	SA9	ISA Adress Bus	O-3,3	PU 8k2 5V	-
60	SYSCLK	ISA Bus Clock (CLK_SYS_ISA)	O-3,3	-	-
61	SA10	ISA Adress Bus	O-3,3	PU 8k2 5V	-
62	REFSH#	ISA System Refresh Control	IO-3,3	PU 1k 5V	-
63	SA11	ISA Adress Bus	O-3,3	PU 8k2 5V	-
64	DREQ1	ISA DMA Request 1	I-3,3	PU 8k2 5V	-
65	SA12	ISA Adress Bus	O-3,3	PU 8k2 5V	-
66	DACK1#	ISA DMA Acknowledge 1	IO-3,3	-	-
67	GND	Ground	PWR	-	-
68	GND	Ground	PWR	-	-
69	SA13	ISA Adress Bus	O-3,3	PU 8k2 5V	-
70	DREQ3	ISA DMA Request 3	I-3,3	PU 8k2 5V	-
71	SA14	ISA Adress Bus	O-3,3	PU 8k2 5V	-
72	DACK3#	ISA DMA Acknowledge 3	IO-3,3	-	-
73	SA15	ISA Adress Bus	O-3,3	PU 8k2 5V	-
74	IOR#	ISA I/O Read	IO-3,3	PU 8k2 5V	-
75	SA16	ISA Adress Bus	O-3,3	PU 8k2 5V	-
76	IOW#	ISA I/O Write	IO-3,3	PU 8k2 5V	-
77	SA18	ISA Adress Bus	O-3,3	PU 8k2 5V	-
78	SA17	ISA Adress Bus	O-3,3	PU 8k2 5V	-
79	SA19	ISA Adress Bus	O-3,3	PU 8k2 5V	-
80	SMEMR#	ISA System Memory Read	IO-3,3	PU 8k2 5V	-
81	IOCHRDY	ISA I/O Channel Ready	IO-3,3	PU 1k 5V	-
82	AEN	ISA Adress Enable	IO-3,3	-	-
83	VCC	Power +5V	PWR	-	-
84	VCC	Power +5V	PWR	-	-
85	SD0	ISA Data Bus	IO-3,3	PU 8k2 5V	-
86	SMEMW#	ISA System Memory Write	IO-3,3	PU 8k2 5V	-
87	SD2	ISA Data Bus	IO-3,3	PU 8k2 5V	-
88	SD1	ISA Data Bus	IO-3,3	PU 8k2 5V	-
89	SD3	ISA Data Bus	IO-3,3	PU 8k2 5V	-
90	NOWS#	ISA No Wait Staits	I-3,3	PU 8k2 5V	-
91	DREQ2	ISA DMA Request 2	I-3,3	PU 8k2 5V	-
92	SD4	ISA Data Bus	IO-3,3	PU 8k2 5V	-
93	SD5	ISA Data Bus	IO-3,3	PU 8k2 5V	-
94	IRQ9	ISA Interrupt Request 9	I-3,3	PU 8k2 5V	-
95	SD6	ISA Data Bus	IO-3,3	PU 8k2 5V	-
96	SD7	ISA Data Bus	IO-3,3	PU 8k2 5V	-
97	IOCHK#	ISA I/O Channel Check	I-3,3	PU 8k2 5V	-
98	RSTDRV	ISA Reset	O-3,3	-	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

4.4.2 Connector X2 Signal Description

ISA Bus Slot

The implementation of this subsystem complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Restrictions:

Memory Transfer:

According to the used LPC 2 ISA solution only memory transfer in the Firmware HUB memory range and with Firmware HUB commands is possible. The Firmware HUB range is from FED4:0000 to FED4:0FFF

I/O Transfer:

Only two generic decoding ranges are available which can be selected in the BIOS setup with a maximum size of 256 Byte. This works of course only, when there are no other devices connected to that I/O ports in that range.

It can be that there is only one decoding range available, when there are the COM and/or parallel ports of an external SuperI/O controller used.

Signal level:

The signal level of the used Fintec controller is 3,3V, 5V tolerant. To achieve the 5V level, most of the signals are pulled up to 5V.

4.5 Connector X3 (VGA, LCD, Video, COM1 and COM2, LPT/Floppy, Mouse, Keyboard)

Flat-Panel Interfaces

ETX®-CD modules can implement an LVDS flat-panel interface called JUMPtec Intelligent LVDS Interface (JILI). These modules do not implement a parallel digital flat-panel interface called JUMPtec Intelligent Digital Interface (JIDI).

LVDS Interface Pinout (JILI)			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#**	10	DDDA
11	LCDDO16	12	LCDDO18
13	LCDDO17	14	LCDDO19
15	GND	16	GND
17	LCDDO13	18	LCDDO15
19	LCDDO12	20	LCDDO14
21	GND	22	GND
23	LCDDO8	24	LCDDO11

25	LCDDO9	26	LCDDO10
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC *	40	VCC *
41	JILI_DAT	42	LTGIO0**
43	JILI_CLK	44	BLON#
45	BIASON**	46	DIGON
47	COMP**	48	Y**
49	SYNC**	50	C**

Notes: **To protect external power lines of peripheral devices, make sure that:*
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950.
***This signal is not supported on the ETX®-CD.*

Parallel Port / Floppy Interfaces

You can configure ETX®-CD's parallel port interfaces as conventional PC parallel ports or as an interface for a floppy-disk drive. You can select the operating mode in the BIOS settings and by a hardware mode-select pin.

If Pin X3-51 (LPT/FLPY#) is grounded at boot time, the floppy support mode is selected. If the pin is left floating or is held high, parallel-port mode is selected. The mode selection is determined at boot time. It cannot be changed until the next boot cycle.

Parallel Port Mode Pinout					Floppy Support Mode Pinout			
Pin	Signal	Pin	Signal		Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED		51	LPT/FLPY#	52	RESERVED
53	VCC *	54	GND		53	VCC *	54	GND
55	STB#	56	AFD#		55	RESERVED	56	DENSEL
57	RESERVED	58	PD7		57	RESERVED	58	RESERVED
59	IRRX	60	ERR#		59	IRRX	60	HDSEL#
61	IRTX	62	PD6		61	IRTX	62	RESERVED
63	RXD2	64	INIT#		63	RXD2	64	DIR#
65	GND	66	GND		65	GND	66	GND
67	RTS2#	68	PD5		67	RTS2#	68	RESERVED
69	DTR2#	70	SLIN#		69	DTR2#	70	STEP#
71	DCD2#	72	PD4		71	DCD2#	72	DSKCHG#
73	DSR2#	74	PD3		73	DSR2#	74	RDATA#
75	CTS2#	76	PD2		75	CTS2#	76	WP#
77	TXD2	78	PD1		77	TXD2	78	TRKO#
79	RI2#	80	PD0		79	RI2#	80	INDEX#
81	VCC *	82	VCC*		81	VCC *	82	VCC *
83	RXD1	84	ACK#		83	RXD1	84	DRV
85	RTS1#	86	BUSY		85	RTS1#	86	MOT
87	DTR1#	88	PE		87	DTR1#	88	WDATA#

89	DCD1#	90	SLCT#		89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK		91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT		93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK		95	TXD1	96	KBCLK
97	RI1#	98	KBDAT		97	RI1#	98	KBDAT
99	GND	100	GND		99	GND	100	GND

*Notes: *To protect external power lines of peripheral devices, make sure that:*
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.5.1 Connector X3 (Signal Levels)

Pin 1–50: [Power | VGA | LCD | TV]

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	R	Analog Video Out RGB - Red Channel	O	-	-
4	B	Analog Video Out RGB - Blue Channel	O	-	-
5	HSY	Horizontal Synchronization Pulse	O-3,3	-	-
6	G	Analog Video Out RGB - Green Channel	O	-	-
7	VSY	Vertical Synchronization Pulse	O-3,3	-	-
8	DDCK	Display Data Channel Clock	IO-5	PU 2k2 5V	-
9	DETECT#	Panel Hot-Plug Detection	nc	-	not supported
10	DDDA	Display Data Channel Data	IO-5	PU 2k2 5V	-
11	LCDD016	LVDS Channel Data	O	-	-
12	LCDD018	LVDS Channel Data	O	-	-
13	LCDD017	LVDS Channel Data	O	-	-
14	LCDD019	LVDS Channel Data	O	-	-
15	GND	Ground	PWR	-	-
16	GND	Ground	PWR	-	-
17	LCDD013	LVDS Channel Data	O	-	-
18	LCDD015	LVDS Channel Data	O	-	-
19	LCDD012	LVDS Channel Data	O	-	-
20	LCDD014	LVDS Channel Data	O	-	-
21	GND	Ground	PWR	-	-
22	GND	Ground	PWR	-	-
23	LCDD08	LVDS Channel Data	O	-	-
24	LCDD011	LVDS Channel Data	O	-	-
25	LCDD09	LVDS Channel Data	O	-	-
26	LCDD010	LVDS Channel Data	O	-	-
27	GND	Ground	PWR	-	-
28	GND	Ground	PWR	-	-
29	LCDD04	LVDS Channel Data	O	-	-
30	LCDD07	LVDS Channel Data	O	-	-
31	LCDD05	LVDS Channel Data	O	-	-
32	LCDD06	LVDS Channel Data	O	-	-
33	GND	Ground	PWR	-	-
34	GND	Ground	PWR	-	-
35	LCDD01	LVDS Channel Data	O	-	-
36	LCDD03	LVDS Channel Data	O	-	-
37	LCDD00	LVDS Channel Data	O	-	-
38	LCDD02	LVDS Channel Data	O	-	-
39	VCC	Power +5V	PWR	-	-
40	VCC	Power +5V	PWR	-	-
41	JILI_DAT	JILI I2C Data Signal	IO-3,3	PU 2k2 3,3V	-
42	LTGIO0	PWM Brightness control for LCD	O-3,3	-	-
43	JILI_CLK	JILI I2C Clock Signal	IO-3,3	PU 2k2 3,3V	-
44	BLON#	Display Backlight On	O-3,3	-	-
45	BIASON	Display Contrast	nc	-	not supported
46	DIGON	Display Power On	O-3,3	-	-
47	COMP	Composite Video / SCART Blue	O	-	-
48	Y	S-Video Luminance / SCART Red	O	-	-
49	SYNC	-	nc	-	Not supported
50	C	S-Video Chrominance / SCART Green	O	-	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

Pin 51–100: [Power | COM | LPT | Floppy | KB/MS/IR]

Pin	Signal	Description	Type	Termination	Comment
51	LPT | FLPY#	LPT / Floppy Interface Configuration Input	I-5	PU 4k7 5V	High: LPT, Low:
52	nc	-	nc	-	Reserved
53	VCC	Power +5V	PWR	-	-
54	GND	Ground	PWR	-	-
55	STB# | nc	LPT Strobe Signal	O-5	-	-
56	AFD# | DENSEL	LPT Automatic Feed / Floppy Density Select	O-5	-	-
57	nc	-	nc	-	Reserved
58	PD7 | nc	LPT Data Bus D7	IO-5	-	-
59	IRRX	Infrared Receive	I-5	-	-
60	ERR# | HDSEL#	LPT Error / Floppy Head Select	IO-5	-	-
61	IRTX	Infrared Transmit	O-5	-	-
62	PD6 | nc	LPT Data Bus D6	IO-5	-	-
63	RXD2	Data Receive COM2	I-5	PU 100k 5V	-
64	INIT# | DIR#	LPT Initiate / Floppy Direction	O-5	-	-
65	GND	Ground	PWR	-	-
66	GND	Ground	PWR	-	-
67	RTS2#	Request to Send COM2	O-5	PU 100k 5V	-
68	PD5 | nc	LPT Data Bus D5	IO-5	-	-
69	DTR2#	Data Terminal Ready COM2	O-5	PU 100k 5V	-
70	SLIN# | STEP#	LPT Select / Floppy Motor Step	O-5	-	-
71	DCD2#	Data Carrier Detect COM2	I-5	PU 100k 5V	-
72	PD4 | DSKCHG#	LPT Data Bus D4 / Floppy Disk Change	IO-5	-	-
73	DSR2#	Data Set Ready COM2	I-5	PU 100k 5V	-
74	PD3 | RDATA#	LPT Data Bus D3 / Floppy Raw Data Read	IO-5	-	-
75	CTS2#	Clear to Send COM2	I-5	PU 100k 5V	-
76	PD2 | WP#	LPT Data Bus D2 / Floppy Write Protect Signal	IO-5	-	-
77	TXD2	Data Transmit COM2	O-5	PU 100k 5V	Bootstrap PU 4k7
78	PD1 | TRK0#	LPT Data Bus D1 / Floppy Track Signal	IO-5	-	-
79	RI2#	Ring Indicator COM2	I-5	PU 100k 5V	-
80	PD0 | INDEX#	LPT Data Bus D0 / Floppy Index Signal	IO-5	-	-
81	VCC	Power +5V	PWR	-	-
82	VCC	Power +5V	PWR	-	-
83	RXD1	Data Receive COM1	O-5	PU 100k 5V	-
84	ACK# | DRV	LPT Acknowledge / Floppy Drive Select	IO-5	-	-
85	RTS1#	Request to Send COM1	O-5	PU 100k 5V	Bootstrap PU 4k7
86	BUSY# | MOT	LPT Busy / Floppy Motor Select	IO-5	-	-
87	DTR1#	Data Terminal Ready COM1	O-5	PU 100k 5V	Bootstrap PU 4k7
88	PE | WDATA#	LPT Paper Empty / Floppy Raw Write Data	IO-5	-	-
89	DCD1#	Data Carrier Detect COM1	I-5	PU 100k 5V	-
90	SLCT#|WGATE#	LPT Power On / Floppy Write Enable	IO-5	-	-
91	DSR1#	Data Set Ready COM1	I-5	PU 100k 5V	-
92	MSCLK	Mouse Clock	O-5	PU 4k7 5V	-
93	CTS1#	Clear to Send COM1	I-5	PU 100k 5V	-
94	MSDAT	Mouse Data	IO-5	PU 4k7 5V	-
95	TXD1	Data Transmit COM1	O-5	PU 100k 5V	Bootstrap PU 4k7
96	KBCLK	Keyboard Clock	O-5	PU 4k7 5V	-
97	RI1#	Ring Indicator COM1	I-5	PU 100k 5V	-
98	KBDAT	Keyboard Data	IO-5	PU 4k7 5V	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

4.5.2 Connector X3 Signal Description

VGA Output

LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Digital Flat Panel Interface (JIDI)

The ETX®-CD does not support the JUMPtec Intelligent Digital Interface (JIDI).

Serial Ports (1 and 2)

The ETX®-CD supports two serial interfaces (TTL). You can use COM2 for IrDA SIR operation. This feature is implemented in the super I/O device, which is a Winbond 83627HF.

The implementation of the serial interface complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Configuration:

The serial-communication interface uses I/O and IRQ resources. The resources are allocated by the BIOS during POST configuration and are set to be compatible with common PC/AT settings. Use the BIOS setup to change some parameters that relate to the serial-communication interface.

PS/2 Keyboard

The implementation of the keyboard interface complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Configuration:

The keyboard uses I/O and IRQ resources. The BIOS allocates the resources during POST configuration. The resources are set to be compatible with common PC/AT settings. Use the BIOS setup to change some keyboard-related parameters.

PS/2 Mouse

The implementation of the mouse interface complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Configuration:

The mouse uses I/O and IRQ resources. The BIOS allocates the resources during POST configuration. The resources are set to be compatible with common PC/AT settings. You can change some mouse-related parameters from the BIOS setup.

IrDA

The ETX®-CD is capable of IrDA SIR operation. This feature is implemented in the Winbond 83627HF. Contact Kontron Embedded Systems for help with this feature.

Parallel Port

The parallel-communication interface shares signals with the floppy-disk interface. The implementation of this parallel port complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Configuration:

The parallel-communication interface uses I/O, IRQ, and DMA resources. The resources are allocated by the BIOS during POST configuration and are set to be compatible with common PC/AT settings. You can change some parameters of the parallel-communication interface through the BIOS setup.

Floppy

The floppy-disk interface shares signals with the parallel-communication interface. The floppy interface is limited to one drive (drive_1). A standard floppy cable has two connectors for floppy drives. One connector has a non-twisted cable leading to it, the other has a twisted cable leading to it. When using the floppy interface you must connect the floppy drive to the connector (drive_1) that has the non-twisted cable leading to it.

The implementation of this subsystem complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Configuration:

The floppy-disk controller uses I/O, IRQ, and direct memory access (DMA) resources. These resources are allocated by BIOS during POST configuration and are compatible with common PC/AT settings. You can change some parameters of the parallel-communication interface through the BIOS setup.

4.6 Connector X4 Subsystems

4.6.1 Connector X4 (IDE 1, IDE 2, Ethernet, Miscellaneous)

Pin	Signal	Pin	Signal		Pin	Signal	Pin	Signal
1	GND	2	GND		51	SIDE_IOW#**	52	PIDE_IOR#
3	5V_SB	4	PWGIN		53	SIDE_DRQ**	54	PIDE_IOW#
5	PS_ON	6	SPEAKER		55	SIDE_D15**	56	PIDE_DRQ
7	PWRBTN#	8	BATT		57	SIDE_D0**	58	PIDE_D15
9	KBINH#	10	LILED#		59	SIDE_D14**	60	PIDE_D0
11	RSMRST#	12	ACTLED#		61	SIDE_D1**	62	PIDE_D14
13	ROMKBCS#**	14	SPEEDLED#		63	SIDE_D13**	64	PIDE_D1
15	EXT_PRG**	16	I2CLK		65	GND	66	GND
17	VCC*	18	VCC*		67	SIDE_D2**	68	PIDE_D13
19	OVCR#	20	GPCS#**		69	SIDE_D12**	70	PIDE_D2
21	EXTSMI#	22	I2DAT		71	SIDE_D3**	72	PIDE_D12
23	SMBCLK	24	SMBDATA		73	SIDE_D11**	74	PIDE_D3
25	SIDE_CS3#**	26	RESERVED		75	SIDE_D4**	76	PIDE_D11
27	SIDE_CS1#**	28	DASP_S**		77	SIDE_D10**	78	PIDE_D4
29	SIDE_A2**	30	PIDE_CS3#		79	SIDE_D5**	80	PIDE_D10
31	SIDE_A0**	32	PIDE_CS1#		81	VCC	82	VCC
33	GND	34	GND		83	SIDE_D9**	84	PIDE_D5
35	PDIAG_S**	36	PIDE_A2		85	SIDE_D6**	86	PIDE_D9
37	SIDE_A1**	38	PIDE_A0		87	SIDE_D8**	88	PIDE_D6
39	SIDE_INTRQ**	40	PIDE_A1		89	RESERVED	90	RESERVED
41	RESERVED	42	RESERVED		91	RXD#	92	PIDE_D8
43	SIDE_AK#**	44	PIDE_INTRQ		93	RXD	94	SIDE_D7
45	SIDE_RDY**	46	PIDE_AK#		95	TXD#	96	PIDE_D7
47	SIDE_IOR#**	48	PIDE_RDY		97	TXD	98	HDRST#
49	VCC*	50	VCC*		99	GND	100	GND

Notes: *To protect external power lines of peripheral devices, make sure that:*
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950
***This signal is not supported on the ETX®-CD.*

4.6.2 Connector X4 (Signal Levels)

Pin 1–50: [Power | IDE | Ethernet | Power control | Misc]

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	5V_SB	Supply of internal suspend Circuit	I	-	-
4	PWGIN	Power Good / Reset Input	I	-	-
5	PS_ON	Power Supply On	O-3,3	PU 10k 3,3V	-
6	SPEAKER	Speaker Output	O-3.3	-	int. PD 20k (ICH7-M)
7	PWRBTN#	Power Button	I-3,3	PU 4k7 3,3V	-
8	BATT	Battery Supply	I	-	-
9	KBINH	Keyboard Inhibit Control Input	I-5	-	-
10	LILED	Ethernet Link LED	O-3,3	-	-
11	RSMRST#	Resume Reset	nc	PU 10k 3,3V	Not supported
12	ACTLED	Ethernet Activity LED	O-3,3	-	-
13	ROMKBCS#	-	nc	-	not supported
14	SPEEDLED	Ethernet Speed LED	O-3,3	-	on at 100Mb/s
15	EXT_PRG	-	nc	-	not supported
16	I2CLK	I2C Bus Clock	O-5	PU 2k2 5V	-
17	VCC	Power +5V	PWR	-	-
18	VCC	Power +5V	PWR	-	-
19	OVCR#	Over Current Detect for USB	I-3,3	PU 10k 3,3V	-
20	GPCS#	-	nc	-	not supported
21	EXTSMI#	System Management Interrupt Input	I-3,3	PU 10k 3,3V	-
22	I2DAT	I2C Bus Data	IO-5	PU 2k2 5V	-
23	SMBCLK	SM Bus Clock	O-3,3	PU 2k2 3,3V	-
24	SMBDATA	SM Bus Data	IO-3,3	PU 2k2 3,3V	-
25	SIDE_CS3#	-	nc	-	not supported
26	SMBALERT	SMB Alert	I-3,3	PU 2k2 3,3V	-
27	SIDE_CS1#	-	nc	-	-
28	DASP_S	-	nc	-	not supported
29	SIDE_A2	-	nc	-	-
30	PIDE_CS3#	Primary IDE Chip Select Channel 1	O-3,3	-	-
31	SIDE_A0	-	nc	-	-
32	PIDE_CS1#	Primary IDE Chip Select Channel 0	O-3,3	-	-
33	GND	Ground	PWR	-	-
34	GND	Ground	PWR	-	-
35	PDIAG_S	-	nc	-	-
36	PIDE_A2	Primary IDE Adress Bus	O-3,3	-	-
37	SIDE_A1	-	nc	-	-
38	PIDE_A0	Primary IDE Adress Bus	O-3,3	-	-
39	SIDE_INTRQ	-	nc	-	-
40	PIDE_A1	Primary IDE Adress Bus	O-3,3	-	-
41	PM_BATLOW#	Battery Low	I-3,3	PU 8k2 3,3V	-
42	GPE1#	General Purpose Power Event 1	I-3,3	PU 10k 3,3V	GPIO13 on ICH7-M
43	SIDE_AK#	-	nc	-	-
44	PIDE_INTRQ	Primary IDE Interrupt Reqeuest	I-3,3	PU 8k2 3,3V	-
45	SIDE_RDY	-	nc	-	-
46	PIDE_AK#	Primary IDE DMA Acknowledge	O-3,3	-	-
47	SIDE_IOR#	-	nc	-	-
48	PIDE_RDY	Primary IDE Ready	I-3,3	PU 4k7,3V	-
49	VCC	Power +5V	PWR	-	-
50	VCC	Power +5V	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

Pin 51-100: [Power | IDE | Ethernet | Misc]

Pin	Signal	Description	Type	Termination	Comment
51	SIDE_IOW#	-	nc	-	-
52	PIDE_IOR#	Primary IDE IO Read	O-3,3	-	-
53	SIDE_DRQ	-	nc	-	-
54	PIDE_IOW#	Primary IDE IO Write	O-3,3	-	-
55	SIDE_D15	-	nc	-	-
56	PIDE_DRQ	Primary IDE DMA Request	I-3,3	PU 11k5 3,3V	-
57	SIDE_D0	-	nc	-	-
58	PIDE_D15	Primary IDE Data Bus	IO	-	-
59	SIDE_D14	-	nc	-	-
60	PIDE_D0	Primary IDE Data Bus	IO	-	-
61	SIDE_D1	-	nc	-	-
62	PIDE_D14	Primary IDE Data Bus	IO	-	-
63	SIDE_D13	-	nc	-	-
64	PIDE_D1	Primary IDE Data Bus	IO	-	-
65	GND	Ground	PWR	-	-
66	GND	Ground	PWR	-	-
67	SIDE_D2	-	nc	-	-
68	PIDE_D13	Primary IDE Data Bus	IO	-	-
69	SIDE_D12	-	nc	-	-
70	PIDE_D2	Primary IDE Data Bus	IO	-	-
71	SIDE_D3	-	nc	-	-
72	PIDE_D12	Primary IDE Data Bus	IO	-	-
73	SIDE_D11	-	nc	-	-
74	PIDE_D3	Primary IDE Data Bus	IO	-	-
75	SIDE_D4	-	nc	-	-
76	PIDE_D11	Primary IDE Data Bus	IO	-	-
77	SIDE_D10	-	nc	-	-
78	PIDE_D4	Primary IDE Data Bus	IO	-	-
79	SIDE_D5	-	nc	-	-
80	PIDE_D10	Primary IDE Data Bus	IO	-	-
81	VCC	Power +5V	PWR	-	-
82	VCC	Power +5V	PWR	-	-
83	SIDE_D9	-	nc	-	-
84	PIDE_D5	Primary IDE Data Bus	IO	-	-
85	SIDE_D6	-	nc	-	-
86	PIDE_D9	Primary IDE Data Bus	IO	-	-
87	SIDE_D8	-	nc	-	-
88	PIDE_D6	Primary IDE Data Bus	IO	-	-
89	GPE2#	General Purpose Power Event 1	I-3,3	PU 8k2 3,3V	RI of ICH7
90	CBLID_P#	80-conductor IDE cable Channel 0	I-3,3	PD 10k	-
91	RXD#	Ethernet Receive Differential Signal (RXD-)	I	-	121R between
92	PIDE_D8	Primary IDE Data Bus	IO	-	-
93	RXD	Ethernet Receive Differential Signal (RXD+)	I	-	121R between
94	SIDE_D7	-	nc	-	-
95	TXD#	Ethernet Transmit Differential Signal (TXD-)	O	-	100R/C10p between
96	PIDE_D7	Primary IDE Data Bus	IO	-	int. PD 11k5 ICH7-M
97	TXD	Ethernet Transmit Differential Signal (TXD+)	O	-	100R/C10p between
98	HDRST#	Hard Drive Reset	O-5	-	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX® board. Please refer to the design guide for information about additional termination resistors.

4.6.3 Connector X4 Signal Description

IDE Ports

The IDE host adapter is capable of DMA-133 operation and supports only one single IDE channel which is connected to the primary channel of the ETX® connector X4. Per default it is set to DMA-33, to achieve the best compatibility to most baseboard implementations. Implementation information is provided in the ETX® Design Guide. Refer to those documents for additional information.

Configuration:

The IDE host adapter is a PCI bus device. It is configured by the BIOS during PCI device configuration. You can disable it in setup. Resources used by the primary IDE host adapter are compatible with the PC/AT.

Note: PHOENIX BIOS will not recognize a Slave device on an IDE port if there is no Master device connected to the same IDE port. Implementation and limitation information is provided in the ETX® Design Guide from document revision 2.1. Refer to the documentation for additional information.

Ethernet

The Ethernet interface is based on the Intel® 82562 Fast Ethernet PCI controller. This 32-bit PCI controller is a fully integrated 10/100BASE-TX LAN solution.

The Ethernet interface requires an external transformer. See the ETX® Design Guide for suggestions on transformer selection.

Configuration:

The Ethernet interface is a PCI device. The BIOS setup automatically configures it during configuration of the PCI device.

Note: Implementation and limitation information is provided in the ETX® Design Guide from document revision 2.1. Refer to the documentation for additional information.

Power Control

Power Good / Reset Input:

The ETX®-CD provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Power Management

ATX PS Control:

The ETX®-CD can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

External SMI Interrupt

Contact Kontron Embedded Modules GmbH technical support for information on this feature.

Miscellaneous Circuits

Speaker

The implementation of the speaker output complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

Battery

The implementation of the battery input complies with the ETX® Specification. Implementation information is provided in the ETX® Design Guide. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

The I2C Bus is implemented by using general purpose I/O.

You also can access the I2C Bus via JUMPtec's Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the ETX® Design Guide, I2C application notes and JIDA specifications which are available at the Kontron Web site.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the southbridge (Intel 82801GBM) device. For more information about the SM bus, please see the System Management (SM) Bus section in the Appendix A: System Resources chapter.

4.7 Feature Connector J11

4.7.1 SDVO Output

The ETX®-CD Serial Digital Video Out port is integrated in the Intel® 945GM northbridge. It has the following features:

- Serial Digital Video Out Port (SDVOB & SDVOC) support
- Two 12-bit channels
- The SDVO B/C ports can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

The SDVO interface is currently not supported

4.7.2 SDVO Connector and Flat Foil Cable

Connector and flat foil cable information for the SDVO connector (J11) located on the bottom side.

Flat Foil Cable

- YOUNGSHIN MCAB45x150B05

- 45pos,150 mm length, 0.5mm pitch, both ends opposite sides

Connector

- Hirose - FH12-45S-0.5SH
- 0.50mm (.020") Pitch FFC/FPC Connector, Horizontal Right Angle, SMT, 45 Circuits

4.7.3 BIOS Requirements

There is currently no support for this feature!

4.7.4 Pinout Feature Connector J11

Pin	Pin on ETX®-CD	Description
1	GND1	Ground
2	SDVOC_CLKN	Channel C; Clock negative
3	SDVOC_CLKN	Channel C; Clock positive
4	GND2	Ground
5	SDVOC_GREENN	Channel C; Green negative
6	SDVOC_GREENP	Channel C; Green positive
7	GND3	Ground
8	SDVOB_CLKN	Channel B; Clock negative
9	SDVOB_CLKN	Channel B; Clock positive
10	GND4	Ground
11	SDVOB_GREENN	Channel B; Green negative
12	SDVOB_GREENP	Channel B; Green positive
13	GND5	Ground
14	SDVOC_INTN	Channel C; Interrupt negative
15	SDVOC_INTP	Channel C; Interrupt positive
16	GND6	Ground
17	SDVOB_INTN	Channel B; Interrupt negative
18	SDVOB_INTP	Channel B; Interrupt positive
19	GND7	Ground
20	SDVOC_BLUEN	Channel C; Blue negative
21	SDVOC_BLUEP	Channel C; Blue positive
22	GND8	Ground
23	SDVOC_REDN	Channel C; Red negative
24	SDVOC_REDP	Channel C; Red positive
25	GND9	Ground
26	SDVOB_BLUEN	Channel B; Blue negative
27	SDVOB_BLUEP	Channel B; Blue positive
28	GND10	Ground
29	SDVOB_REDN	Channel B; Red negative
30	SDVOB_REDP	Channel B; Red positive
31	GND11	Ground
32	SDVO_FLDSTALLN	Field Stall negative
33	SDVO_FLDSTALLP	Field Stall positive
34	GND12	Ground
35	SDVO_TVCLKINN	TV Clock Input negative
36	SDVO_TVCLKINP	TV Clock Input positive
37	GND13	Ground
38	SDVO_CTRCLK	I2C based control signal for SDVO devices; clock
39	SDVO_CTRLDATA	I2C based control signal for SDVO devices; data
40	RESET#	Reset signal
41	VCC	5V power
42	VCC	5V power
43	VCC	5V power

44	Reserved	nc
45	Reserved	nc

5 Special Features

5.1 Watchdog Timer

This feature is implemented in the Winbond 83627HF super I/O. You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API (Refer to Appendix F: JIDA Standard). The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- 1-second increments from 1 to 255 seconds
- 1-minute increments from 1 to 255 minutes

Contact Kontron Embedded Modules technical support for information on programming and operating the WDT.

6 Design Considerations

6.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules GmbH for the ETX®-CD. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as an ETX®-standard thermal interface to use with a heat sink or other cooling device.

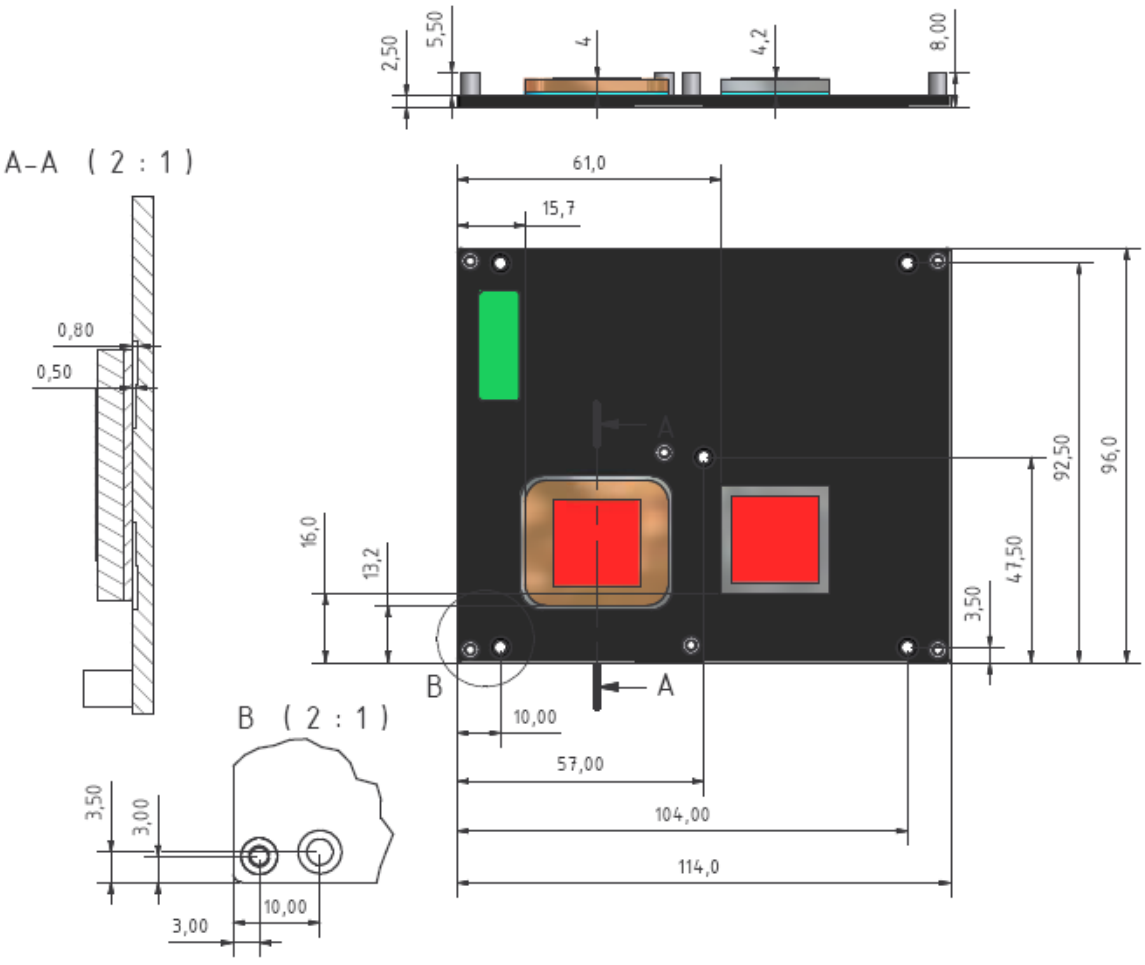
External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60°C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the ETX®-CD. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the ETX® application and environmental conditions. Please see the ETX® Design Guide for further information on thermal management.

6.2 Heatspreader Dimensions

This is the backside view of the heatspreader plate.



Article numbers:

18030-0000-99-0: Heatspreader ETX®-CD, Threaded Hole Stand Off

18030-0000-99-1: Heatspreader ETX®-CD, Through Hole Stand Off

7 Important Technology Information

The following technological information is designed to give the reader a better understanding of some of features of the ETX®-CD. This information can be referenced when reading the System Resources and BIOS Operation sections that follow. There are also references to additional documentation that will help to develop a better understanding of the technical information described herein.

7.1 I/O APIC vs 8259 PIC Interrupt mode

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently then the 8259 PIC. The following information explains these differences. The ETX®-CD only supports the APIC mode of interupt handling.

7.1.1 Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus and interrupts are handled without the needs for the processor to run an interrupt acknowledge cycle.

7.1.2 Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

7.1.3 More interrupts

The I/O APIC in the chipset of the ETX®-CD supports a total of 24 interrupts.

The APIC is not supported by all operating systems. Only Windows Xp supports APIC.

For more information see chapter 8 of the IA-32 Intel Architecture Software Developer's Manual, Volume 3.

7.2 Thermal Monitor and Catastrophic Thermal Protection

The Thermal Monitor within the Intel® processors helps to control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel® Thermal Monitor activates the TCC is not user-configurable and is not software visible.

The Thermal Monitor controls the processor temperature by modulating (starting and stopping) the CPU core clocks at a 50% duty cycle (TM1) or by initiating an Enhanced Intel SpeedStep technology transition (TM2)* when the processor silicon reaches its maximum operating temperature (selectable in setup).

Note: TM2 is the recommended mode for the Intel® Core Duo® and Core2Duo® processors.
**Not supported on the ETX®-CD with the CM 423.*

Thermal Monitor supports two modes to activate the TCC: Automatic and On-Demand mode. The Intel Thermal Monitor Automatic Mode must be enabled via BIOS for the processor to be operating within specification.

Automatic mode does not require any additional hardware, software drivers, or interrupt handling routines.

Note: With a properly designed thermal solution, the TCC is only active for very short periods, hence processor performance impact is expected to be so minor that it would not be detectable.

The Intel® Core Duo® and Core2Duo® processors support the THERMTRIP# signal for catastrophic thermal protection.

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the system BUS signal THERMTRIP# will go active.

THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

7.2.1 Summary

Thermal Control Circuit reduces performance when the processor reaches its max. operating temperature (100°C). THERMTRIP# shuts down the system in case of catastrophic cooling failure.

7.3 Processor Performance Control

The Intel® Core Duo® and Core2Duo® processors run in different performance states (multiple frequency/voltage operating points). The CPU performance can be altered while the computer is functioning. This allows the processor to run at different core frequencies and voltages depending on CPU thermal state and OS policy.

Windows XP includes built-in processor performance control to operate the processor more efficiently when it is not fully utilized. Win2k, WinME and Win9x do not support processor performance control. Special software is required for Oses not capable of processor performance control.

In Windows, the processor performance control policy is linked to the Power Scheme setting in the control panel power option applet.

Note: Windows always runs at the highest performance state when the "Home/Office" or "Always On" power scheme is selected.
For a more detailed information about processor performance control, see:
Chapter 8 of the ACPI Specification Revision 2.0c available at www.acpi.info Windows platform design note at: http://www.microsoft.com/whdc/hwdev/tech/onnow/procperfctrl.mspx

7.4 Thermal Management

ACPI allows the OS to play a role in the thermal management of the system. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system.

The ACPI thermal solution on ETX®-CD supports three cooling policies:

Active Cooling

The OS is turning the fan on/off. Active cooling devices typically consume power and produce noise, but are able to cool a thermal zone without limiting system performance. The active cooling trip point

declares the temperature threshold the OS uses to decide when to start/stop active cooling devices. See section ETX®-CD onboard Fan connectorfor more information about the ETX®-CD onboard Fan control.

Passive Cooling

The OS reduces the power consumption of the processor by throttling the processor clock to reduce the temperature of the thermal zone. Passive cooling devices (processor) produce no noise. The passive cooling trip point declares the temperature threshold where the OS will start or stop passive cooling.

Critical Trip Point

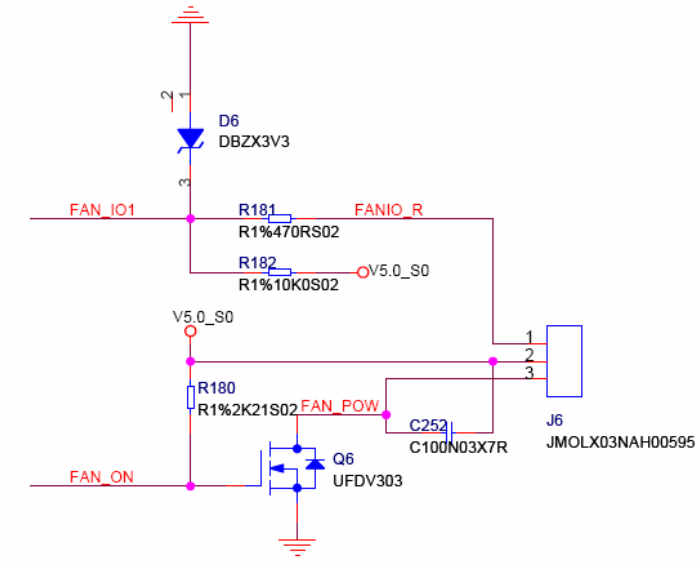
The OS performs an orderly, but critical, shutdown of the system when the temperature reaches the critical trip point.

7.5 ETX®-CD onboard Fan connector

This section describes how to connect a fan to the connector located directly on the ETX®-CD. With certain BIOS-settings it is possible to control the fan depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

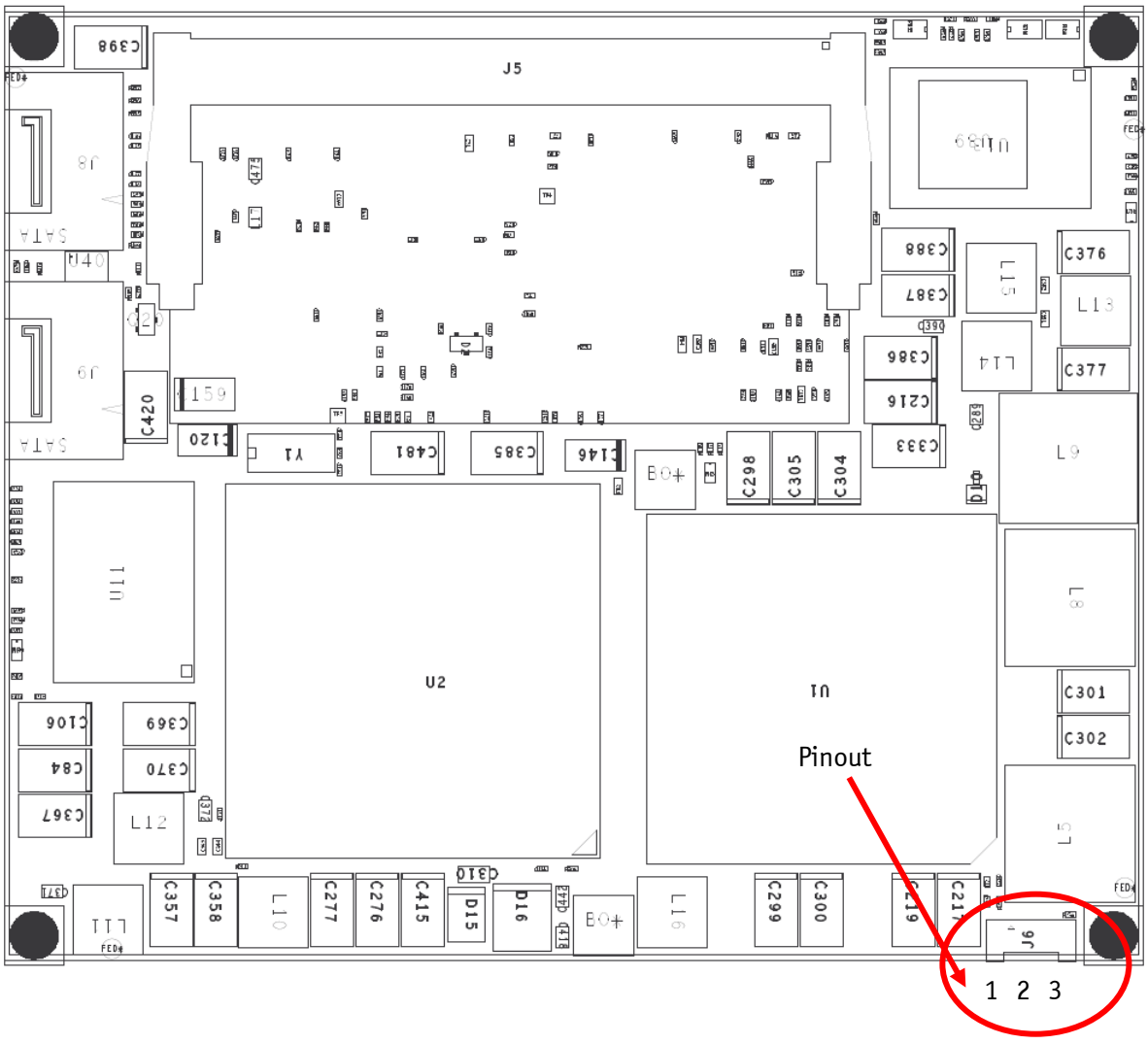
Note: The ETX® CD can not control the revolutions per minute (R.P.M) of the fan.

7.5.1 Schematics of Fan control

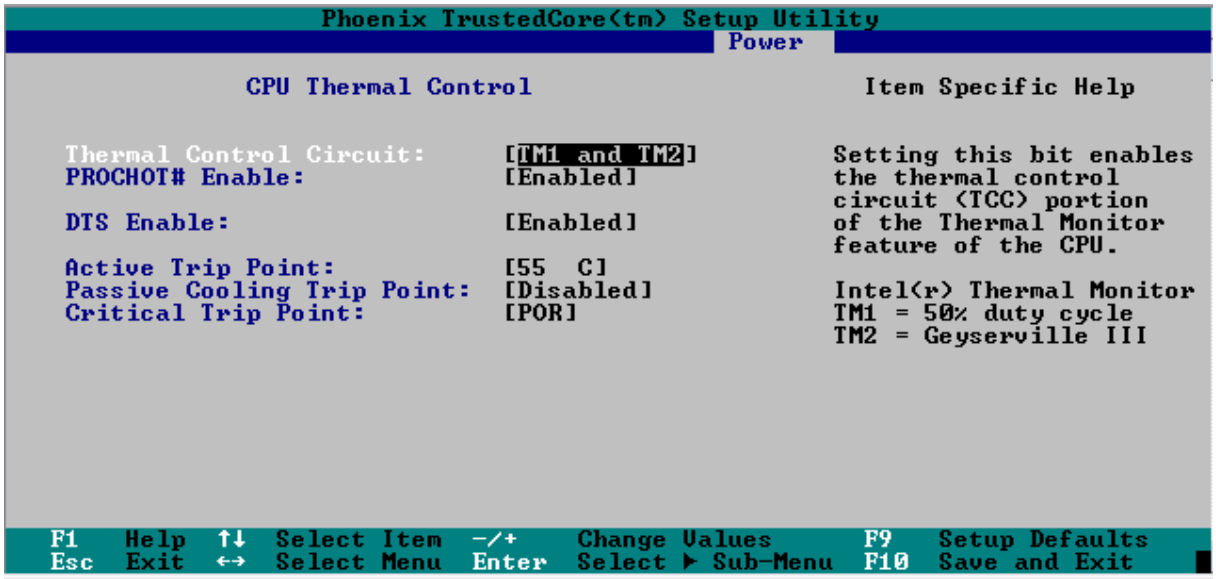


- Part number (Molex) J1: 53261-0390
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

7.5.2 Location and Pinout of Fan connector J6



7.5.3 BIOS Settings



Feature	Option	Description
Active Trip Point	Disabled 15 C 23 C ... **55 C** 63 C ... 119 C	This value controls the temperature of the ACPI active trip point - the point in which the OS will turn on the CPU fan (connector on PCB). If DTS is enabled only values below 97°C are valid.

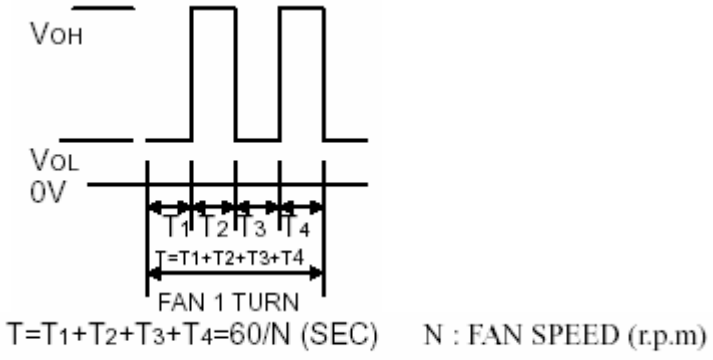
7.5.4 Electrical characteristics

Vcc = 5 V

Imax (continuous) = 0,68 A

Imax (pulsed) = 2 A

Sense (Tacho-pulse) = 4 Pulses per turn

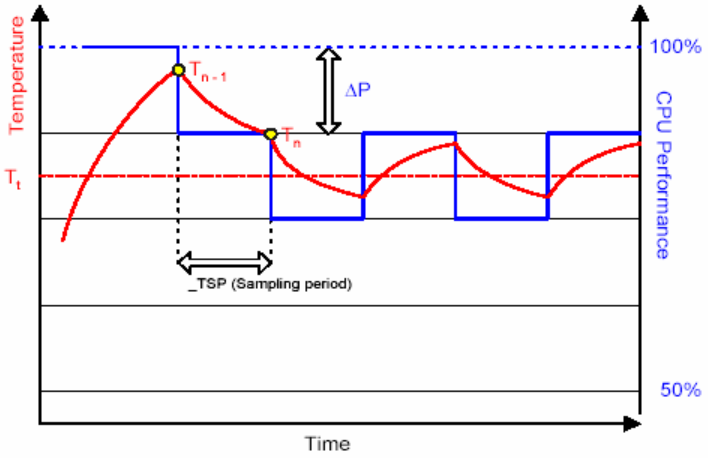


Note: The 5 V output is not short circuit proof. The user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

7.5.5 Processor Clock Throttling

The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation:

ΔP[%] = TC1(Tn-Tn-1) + TC2(Tn-Tt)



ΔP is the performance delta, Tt is the target temperature = passive cooling trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply (setup options section ACPI Control Submenu).

It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

Note: See chapter 12 of the ACPI specification (www.acpi.info) for more details.

7.6 ACPI Suspend Modes and Resume Events

The ETX®-CD, supports the S1 (POS=Power On Suspend) state, S3 and S4.

S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems:

- WinME
- Win2k
- WinXP (S4_OS=Hibernate)

The following events resume the system from S1:

- Power Button
- PS/2 Keyboard and Mouse IRQs (1 & 12)
- USB Wake Events
- PCI Bus signal PME#

The following event resumes the system from S3:

➤ Power Button

8 System Resources

8.1 Interrupt Request (IRQ) Lines

In 8259 PIC mode:

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	LPT2	Yes	Note (2)
6	Floppy Drive Controller	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	No	
10	COM3	Yes	Note (2)
11	COM4	Yes	Note (2)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	SATA	No	Note (3)

Note: 1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
2 Unavailable if baseboard is equipped with an I/O controller SMC FDC37C669, and the device is enabled in setup.
3 Unavailable in SATA legacy mode. It cannot be used for PCI, but for ISA bus, when SATA is in enhanced mode.

In APIC mode:

IRQ #	Used For	Available	Available for PCI	Comment
0	Timer0	No	No	
1	Keyboard	No	No	
2	Slave 8259	No	No	
3	COM2	No	Yes	Note (1)
4	COM1	No	Yes	Note (1)
5	PCI/LPT2	Yes	Yes	Note (2)
6	Floppy Drive Controller	No	Yes	Note (1)
7	LPT1	No	Yes	Note (1)
8	RTC	No	No	
9	SCI	No	No	System Control Interrupt (3)
10	COM3	Yes	Yes	Note (2)
11	COM4	Yes	Yes	Note (2)
12	PS/2 Mouse	No	Yes	Note (1)
13	FPU	No	No	
14	IDE0	No	No	
15	SATA	No	No	Note (3)
16	PIRQ[A]	For PCI		PCI IRQ line 1 + USB UHCI controller #0 + Graphics controller
17	PIRQ[B]	For PCI		PCI IRQ line 2 + AC97 Audio controller + USB UHCI controller #1
18	PIRQ[C]	For PCI		PCI IRQ line 3 + USB UHCI controller #2 + Native IDE
19	PIRQ[D]	For PCI		PCI IRQ line 4 + USB UHCI controller #3
20	PIRQ[E]	No		Lan Controller
21	PIRQ[F]	No		
22	PIRQ[G]	No		
23	PIRQ[H]	No		USB EHCI controller

Note: 1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
2 Unavailable if baseboard is equipped with an I/O controller SMC FDC37C669, and the device is enabled in setup.
3 Unavailable in SATA legacy mode. It cannot be used for PCI, but for ISA bus, when SATA is in enhanced mode.

Warning: The ETX®-CD is always booting in PIC mode. This might lead to the fact, that there are no interrupts for PCI devices available when all onboard and SuperI/O interfaces are enabled. Then the system stops without booting. The only solution is to deactivate interfaces.

8.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0		Yes	
1		Yes	
2	FDC	No	If the "used-for" device is disabled in setup, the corresponding DMA channel is available for other devices.
3	LPT	Yes	Unavailable if LPT is used in ECP mode.
4	Cascade	No	

5		Yes	
6		Yes	
7		Yes	

8.3 Memory Area

Upper Memory	Used for	Available	Comment
C0000h – CFFFFh	VGA BIOS	No	
D0000h – DDFFFh		Yes	shadow RAM (ISA bus restriction)
DE000h – DFFFFh	USB registers	No	
E0000h – FFFFFh	System BIOS	No	

8.4 I/O Address Map

The I/O-port addresses of the ETX®-CD are functionally identical with a standard PC/AT.

The following I/O ports are additionally used:

I/O Address	Used for	Available	Comment
220-227h	COM3		Available if external I/O controller not used.
228-22Fh	COM4		Available if external I/O controller not used.
2F8-2FFh	COM1	No	Available if device is disabled in setup
370-371h	Configuration space for SMC controller	No	Available if external I/O controller not used.
3F8-3FFh	COM2	No	Available if device is disabled in setup
1000h >	PCI	No	I/O ports 1000h and above might be allocated by PCI devices or onboard hardware.

8.5 Peripheral Component Interconnect (PCI) Devices

PCI Device	Busmaster	PCI Interrupt	Comment
Audio, USB and Ethernet		See IRQ resource tables above	Integrated in the Intel chipset. No REQx/GNTx pair needed.

You can use REQ0/GNT0, REQ1/GNT1, REQ2/GNT2, and REQ3/GNT3 pairs for external PCI devices.

8.6 Inter-IC (I2C) Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS data.	0
A2h	JIDA-EEPROM	No		0
B0h	WD-PIC	No	Reserved for internal use.	0

8.7 System Management (SM) Bus

Following SM bus addresses are reserved.

SM Bus Address	SM Device	Comment	JIDA-Bus-Nr.
10h	SMB Host	Do not use under any circumstances.	1
12h	SMART_CHARGER	Not to be used with any SM bus device except a charger	1
14h	SMART_SELECTOR	Not to be used with any SM bus device except a selector	1
16h	SMART_BATTERY	Not to be used with any SM bus device except a battery	1
A0h	SPD	SDRAM EEPROM	1

D2h	Clock generator	Do not use under any circumstances.	1
D4h	Clock generator	Do not use under any circumstances.	1

8.8 JILI-I2C Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JILI-EEPROM	No	EEPROM for JILI-Data	2
62h	Brightness control	No	MAX536262	2

9 Limitations

9.1 ISA Bus

Memory accesses are not supported on the ISA bus. I/O accesses are only supported if they fall into one of the 4 generic decode ranges provided by the chipset. If a plugin ISA card is using registers in I/O space, this address range has to be enabled explicitely using the decode range and size setup items provided under the menu "Advanced" -> "Advanced Chipset Control" -> "ISA Options".

The following devices may also consume a generic decode range which can no longer be used for plugin cards.

"Advanced" -> "I/O device Configuration" -> "SIO Options"

- "External SIO": SIO2 config space, if this range is released (item set to disabled), none of the devices in the external SIO will work
- Serial Port C/D: consumes one range if either one or both COMs are enabled
- External LPT: Consumes one range if enabled

"Advanced" -> "Hardware Monitor"

- "Hardware Monitor": consumes one range if enabled, disable if you don't require HWM support.

Note: the BIOS doesn't check the range and size values set in the ISA Options menu. Ensure that theses values do not conflict with other legacy and PCI I/O resources. Resource conflicts may render the board inoperable. If the number of generic decode ranges is exhausted, a conflict marker will be displayed

9.2 Windows 2000

Windows 2000 can only be installed, when in the BIOS setup ACPI is disable.

10 BIOS Operation

The module is equipped with a Phoenix BIOS, which is located in an onboard Flash EEPROM. The device has 8-bit access. Faster access (16 bit) is provided by the shadow RAM feature. You can update the BIOS using a Flash utility.

10.1 Determining the BIOS Version

To determine the PhoenixBIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

PhoenixBIOS 4.0 Release 6.1

Copyright 1985-2003 Phoenix Technology Ltd

All Rights Reserved

Kontron® BIOS Version <MCALR110>

© Copyright 2002-2007 Kontron Embedded Modules GmbH

10.2 Setup Guide

The PhoenixBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note: Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>. It might also be necessary to use the "reset configuration data" option in the BIOS setup and set it to "yes". In certain circumstances this may also help to recover from system boot failure or a resource conflict.

10.2.1 Start Phoenix BIOS Setup Utility

To start the PhoenixBIOS setup utility, press <F2> when the following string appears during bootup.

Press <F2> to enter Setup

The Main Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

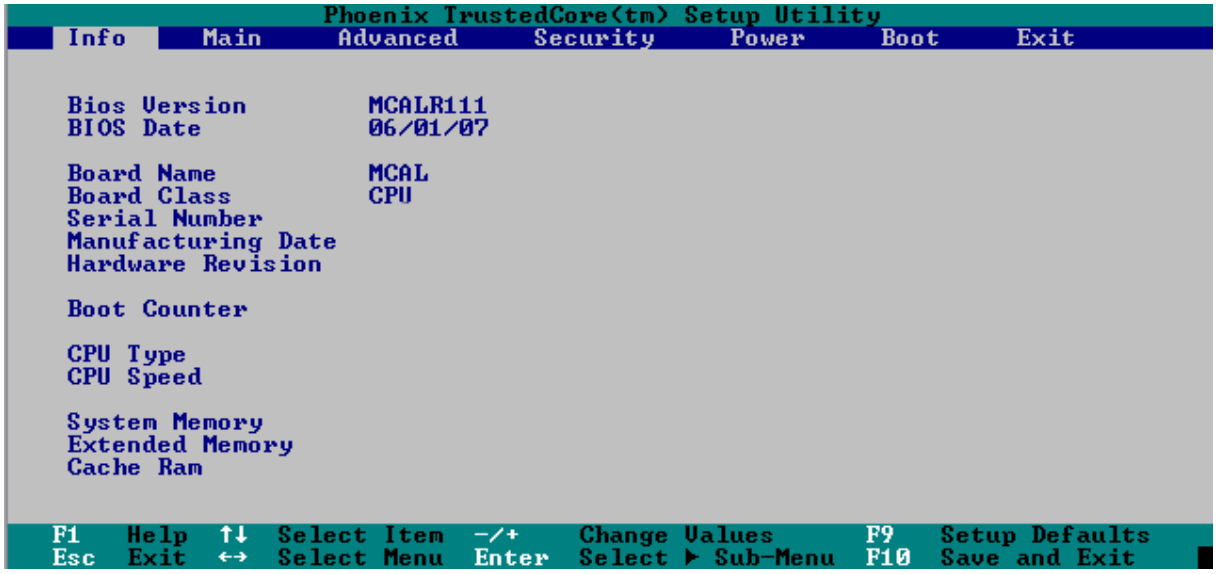
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

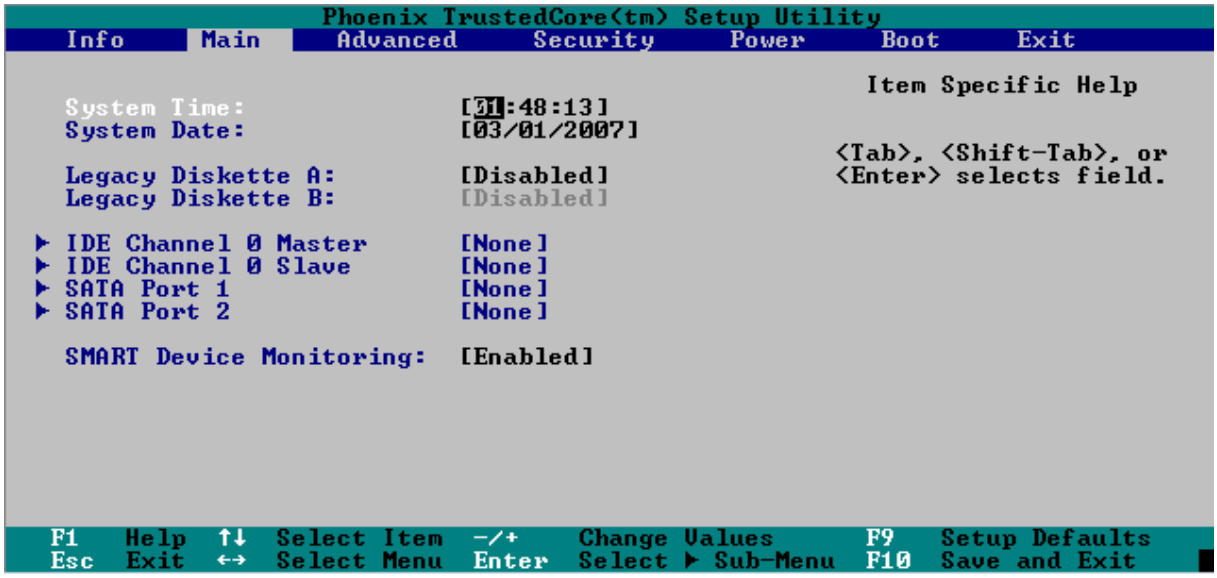
Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

10.3 BIOS Setup Menus

10.3.1 Info Screen

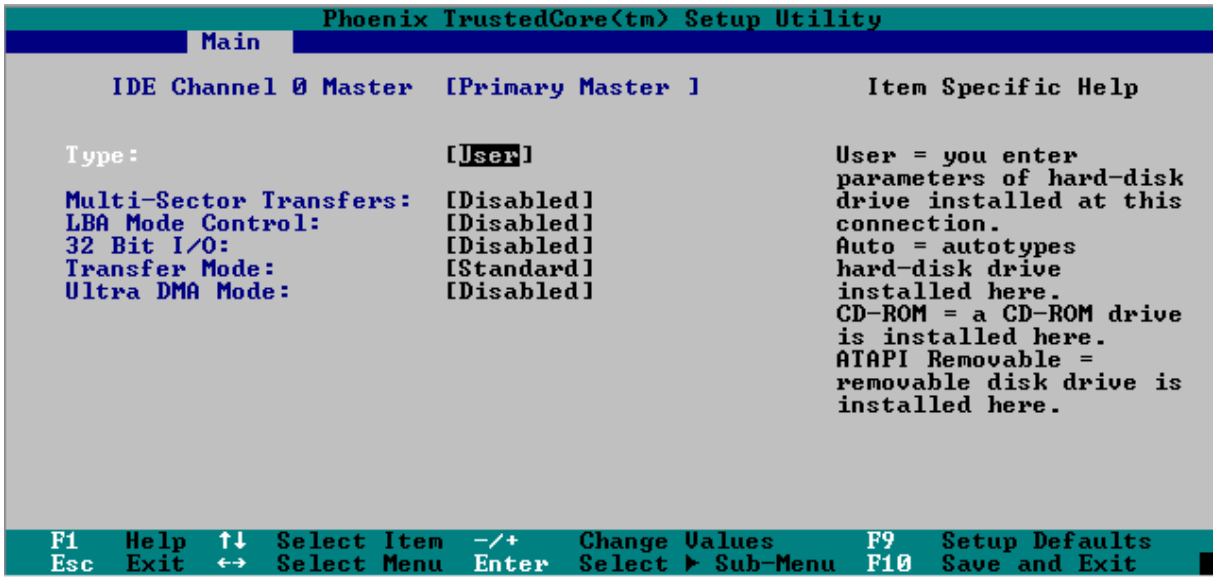


10.3.2 Main Menu



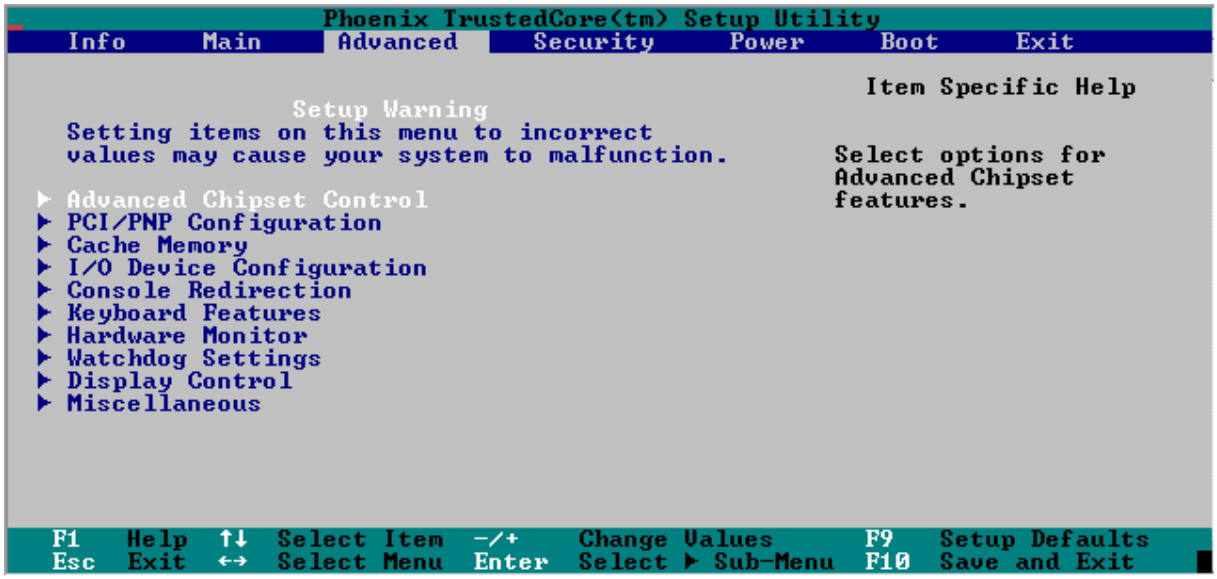
Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field
Legacy Diskette A	**Disabled** 360 kB 1.2 MB 720 kB 1.44 / 1.25 MB 2.88 MB	Selects floppy type. Note that 1.25 MB references a 1024 byte sector Japanese media format. The 1.25 MB MB diskette requires a 3-Mode floppy-disk drive.
Legacy Diskette B	**Disabled** 360 kB 1.2 MB 720 kB 1.44 / 1.25 MB 2.88 MB	
SMART Device Monitoring	**Enabled** Disabled	IDE Failure Prediction

IDE Channels Submenu

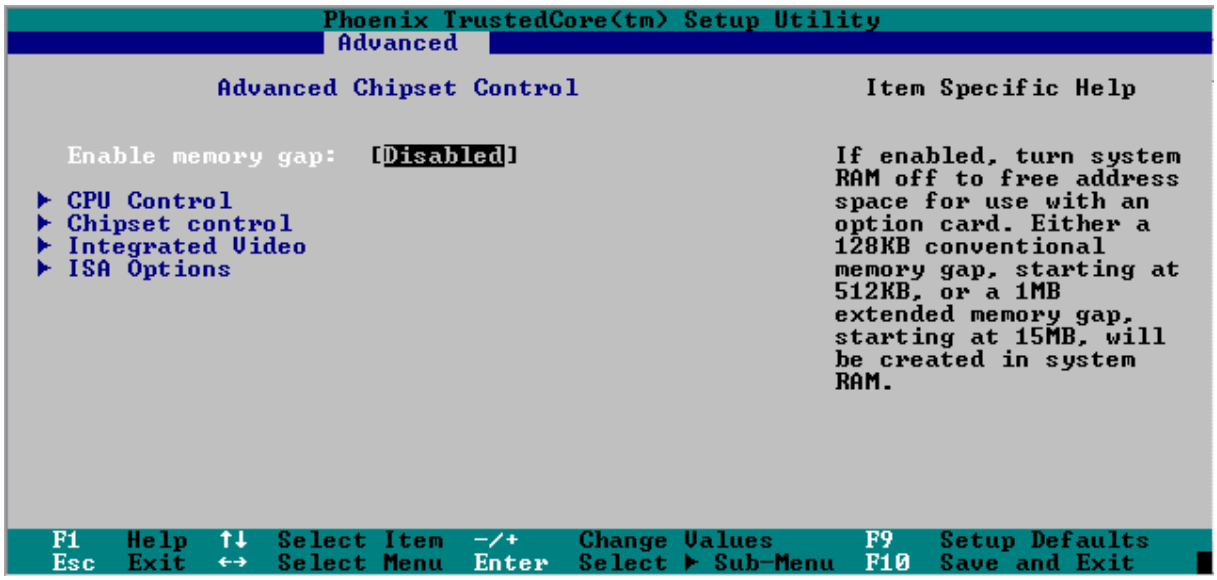


Feature	Option	Description
Type	User **Auto** None ATAPI Removable CD-ROM IDE Removable Other ATAPI	
Multi-Sector Transfers	Disabled 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Specify the number of sectors per block for multiple sector transfers
LBA Mode Control	Disabled Enabled	Enabled LBA causes Logical Block Addressing to be used in place of Cylinders, Heads _Sectors.
32 Bit I/O	**Disabled** Enabled	This setting enables or disables 32 bit data transfers.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.

10.3.3 Advanced



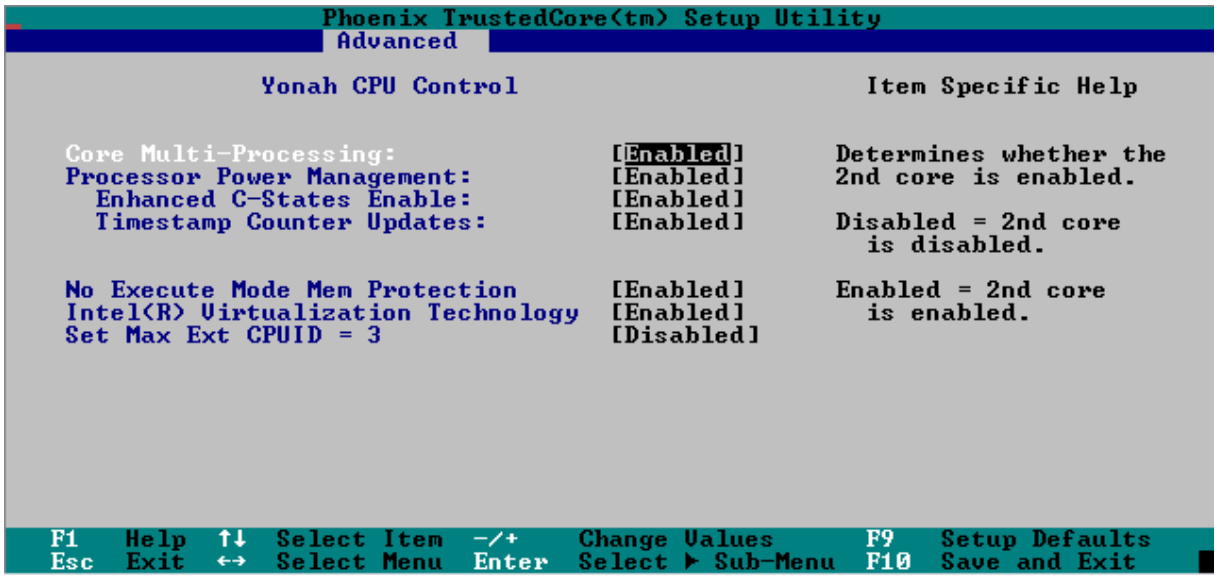
Advanced Chipset Control



Feature	Option	Description
Enable Memory Gap	Enabled **Disabled**	

CPU Control

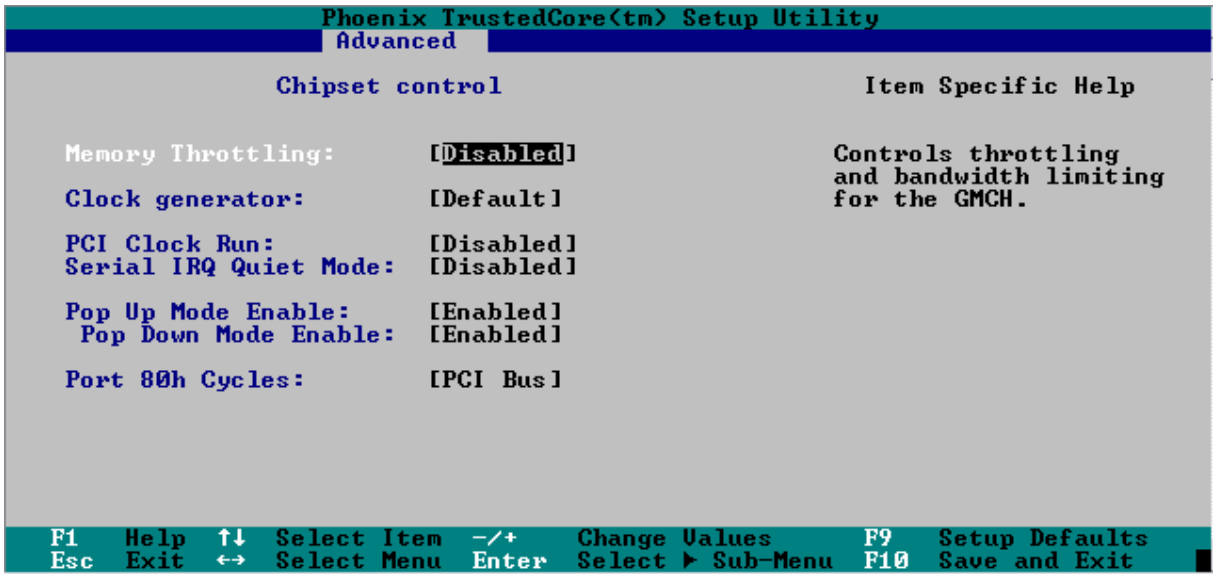
CPU control detects which processor core is used and displays an additional submenu with the detected processor core (yonah, merom, etc.).



Feature	Option	Description
Core Multi-Processing	Enabled Disabled	Enables and disables the 2nd CPU core
Processor Power Management	**Enabled** GV3 only C-states only Disabled	Selects the processor power management
Enhanced C-States Enable	**Enabled** Disabled	Enables enhanced C-states support
Timestamp Counter Updates	**Enabled** Disabled	Control TSC updates after C3/C4 through this setup option
No Execute Mode Mem Protection	**Enabled** Disabled	When disabled, forces the Execute-Disable Bit Capability extended feature bit to always return 0.
Intel® Virtualization Technology	**Enabled** Disabled	When enabled a virtual machine can utilize the additional hardware virtualization capabilities.
Set Max Ext CPUID = 3	Enabled **Disabled**	Set Max CPUID extended function value to 3

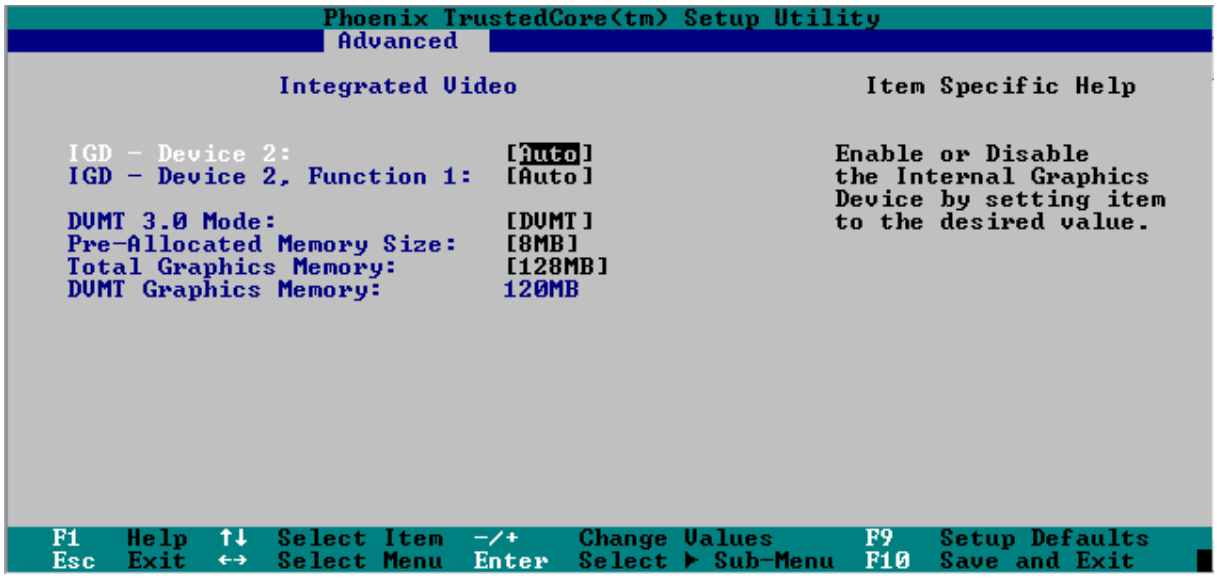
Note: when a Pentium M C423 is in used, then GV3 is not possible and C-States only is the default setting of Processor Power Management

Chipset control



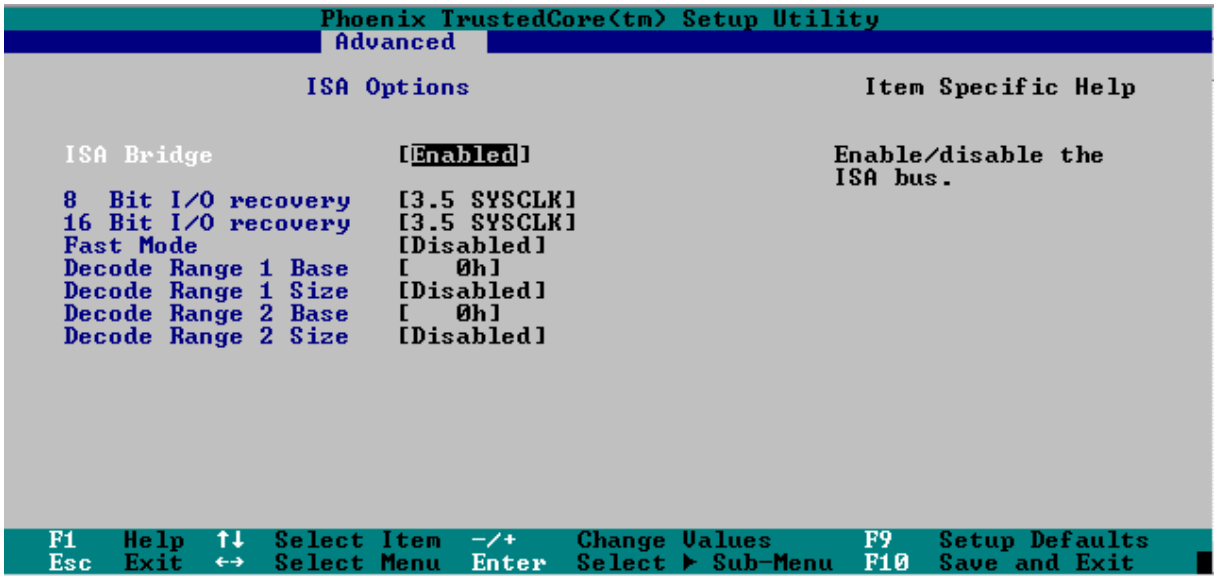
Feature	Option	Description
Memory Throttling	Enabled **Disabled**	Controls throttling and bandwidth limiting for the 945 GME
Clock generator	**Default** Program	"Program" allows to enable/disable manual change of Spread Spectrum and FSB
PCI Clock Run	Enabled **Disabled**	If Enabled the Clock Run logic will stop the PCI clocks
Serial IRQ Quiet Mode	Enabled **Disabled**	Enabled: Quiet Mode for SIRQ Disabled: Continuous Mode for SIRQ Must be enabled for PCI Clock Run enabled
Pop Up Mode Enable	**Enabled** Disabled	Enables/disables C2 and not C0 change when a PCI busmaster event appears
Pop Down Mode Enable	**Enabled** Disabled	Must be switched on when Pop Up Mode is enabled
Port 80 h Cycles	LPC Bus **PCI Bus**	Controls where the port 80 cycles are sent

Integrated Video



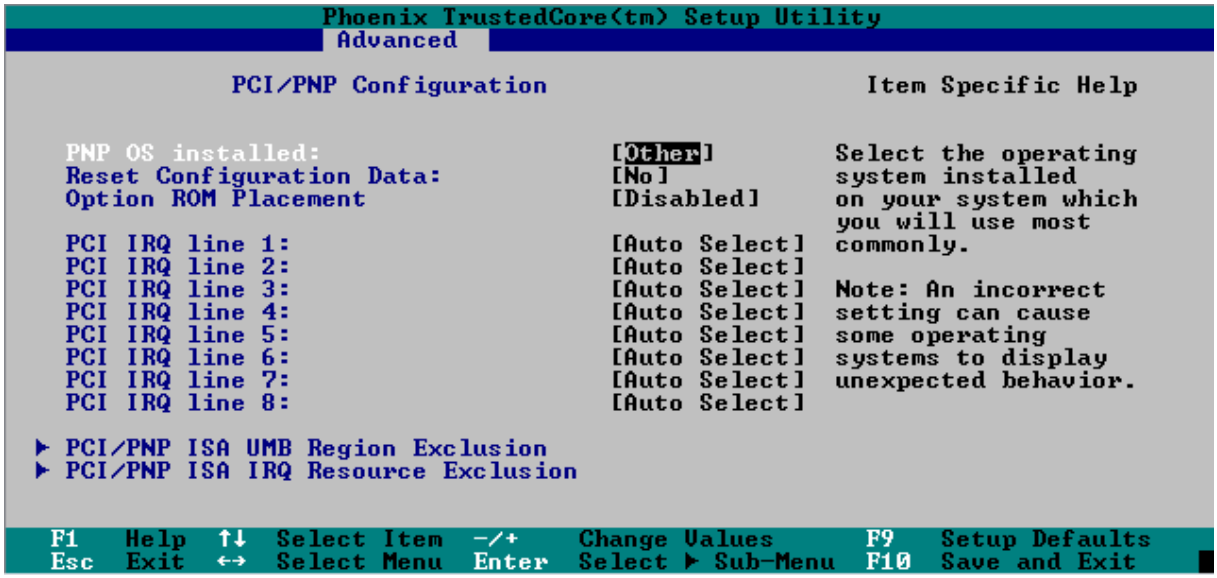
Feature	Option	Description
IGD - Device 2	**Auto** Disabled	
IGD - Device 2, Function 1	**Auto** Disabled	
DVMT 3.0 Mode	Fixed **DVMT** Combo	Selectes the mode of the DMBT graphic memory allocation
Pre-Allocated Memory Size	1 MB **8 MB**	Sets the size of the pre-allocated graphics memory
Total Graphics Memory	**64MB** 128MB maxDVMT	Sets the size of the totals possible graphics memory

ISA Options



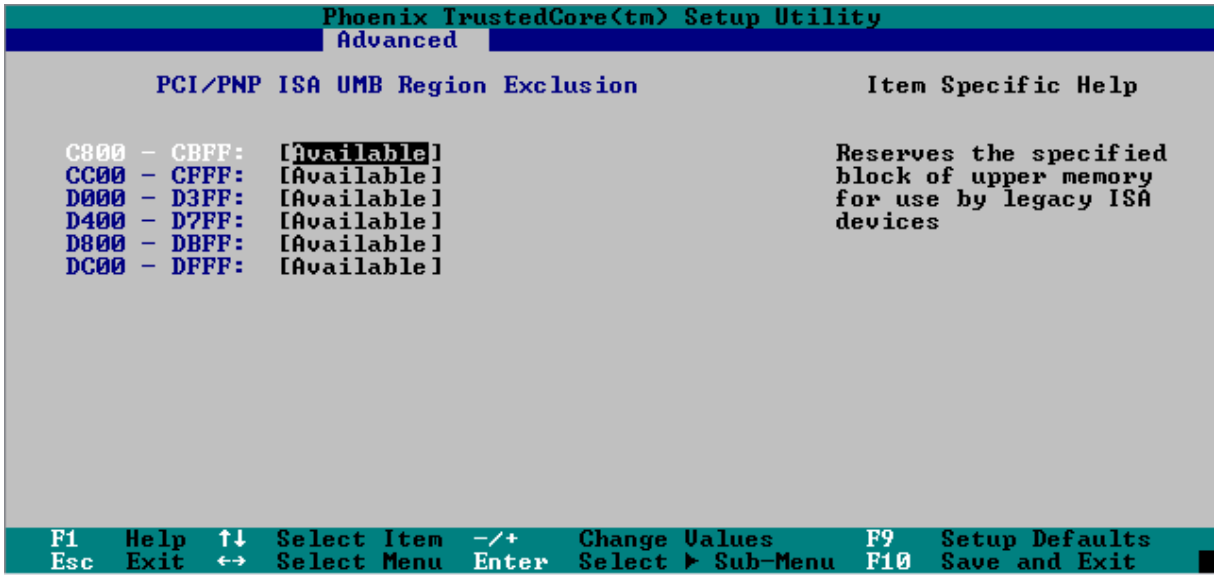
Feature	Option	Description
ISA Bridge	**Enabled** Disabled	Enables/disables the ISA bridge
8 Bit I/O recovery	**3.5 SYSCLK** 4.5 SYSCLK ... 10.5 SYSCLK	Sets the 8 Bit I/O recovery time
16 Bit I/O recovery	**3.5 SYSCLK** 4.5 SYSCLK ... 7.5 SYSCLK	Sets the 16 Bit I/O recovery time
Fast Mode	Ensabled **Disabled**	Enables/disables fast mode (SYSCLK=PCICLK)
Decode Range 1 Base	[0h- FFFFh]	Select I/O Base address for generic decode range
Decode Range 1 Size	**Disabled** 4 8 16 ... 256	Select generic decode range size in bytes
Decode Range 2 Base	[0h- FFFFh]	Select I/O Base address for generic decode range
Decode Range 2 Size	**Disabled** 4 8 16 ... 256	Select generic decode range size in bytes

PCI/PNP Configuration



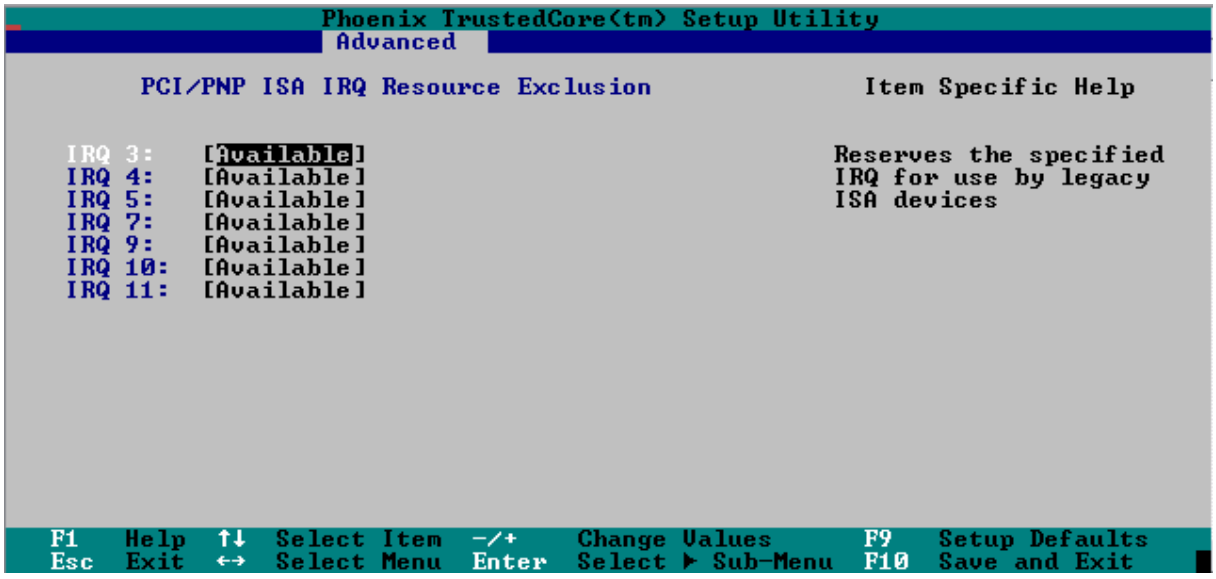
Feature	Option	Description
PNP OS installed	**Other** Win95 Win98 WinMe Win2000 WinXP	Selects the most used OS
Reset Configuration Data	**No** Yes	"Yes" will clear the ESCD
Option ROM Placement	**Disabled** E000 Extension by PFA Temporary Relocation by PFA E000 Extension by Size Temporary Relocation by Size	Sets the mode of option ROM placement
PCI IRQ line 1 PCI IRQ line 2 PCI IRQ line 3 PCI IRQ line 4 PCI IRQ line 5 PCI IRQ line 6 PCI IRQ line 7 PCI IRQ line 8	**Auto Select** 3 4 5 7 10 11 12	PCI devices can use hardware interrupts (IRQs). It can be auto selected when

PCI/PNP ISA UMB Region Exclusion



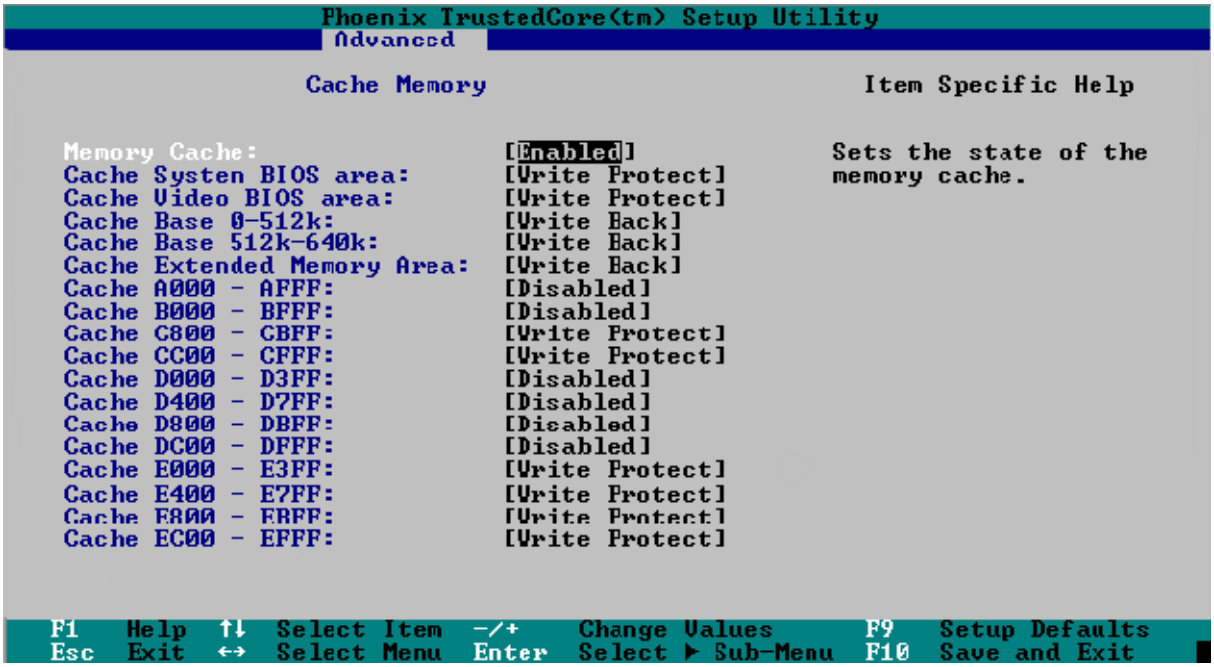
Feature	Option	Description
C000 - CBFF		
CC00 - CFFF		
D000 - D3FF	**Available**	
D400 - D7FF	Reserved	
D800 - DBFF		
DC00 - DFFF		

PCI/PNP ISA IRQ Resource Exclusion



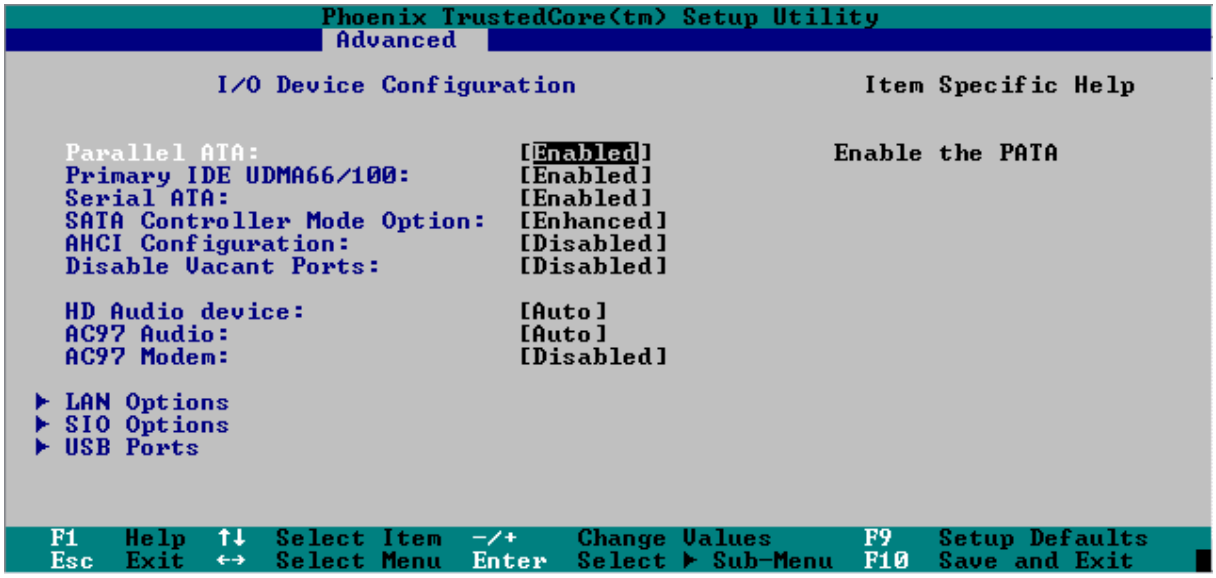
Feature	Option	Description
IRQ 3	**Available** Reserved	
IRQ 4		
IRQ 5		
IRQ 7		
IRQ 9		
IRQ 10		
IRQ 11		

Cache Memory



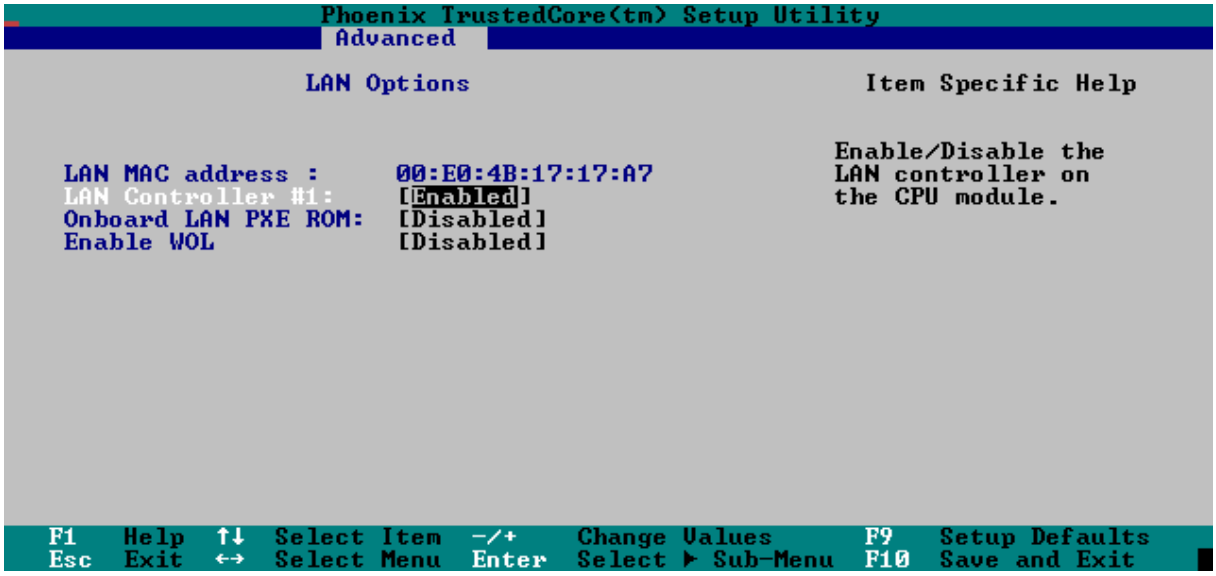
Feature	Option	Description
Memory Cache	**Enabled** Disabled	Enables/disables the memory cache system
Cache System BIOS area	**Write Protect** uncached	Cache setting for System BIOS area
Cache Video BIOS area		Cache setting for System BIOS area
Cache Base 0-512k Cache Base 512k-640k Cache Extended Memory Area	Uncached Write Through Write Protect **Write Back**	Uncached = Disabled: This block is not cached at all USWC Caching: Uncached Speculative Write Combined Write Through: Writes are cached and send to main memory at once Write Protect: Writes are ignored Write Back: Writes are cached, but not sent to main memory until necessary
Cache A000 - AFFF Cache B000 - BFFF	**Disabled** USWC Caching Write Through Write Protect Write Back	
Cache C800 - CBFF Cache CC00 - CFFF	Disabled Write Through **Write Protect** Write Back	
Cache D000 - D3FF Cache D400 - D7FF Cache D800 - DBFF Cache DC00 - DFFF	**Disabled** Write Through Write Protect Write Back	
Cache E000 - E3FF Cache E400 - E7FF Cache E800 - EBFF Cache EC00 - EFFF	Disabled Write Through **Write Protect** Write Back	

I/O Device Configuration



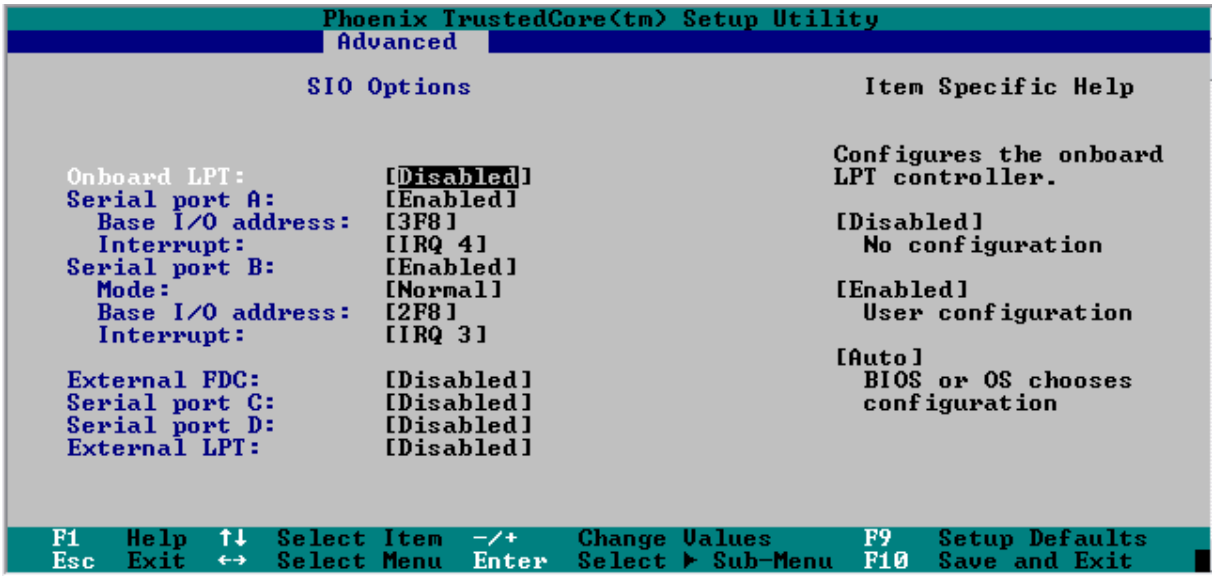
Feature	Option	Description
Parallel ATA	**Enabled** Disabled	Enables/disables the PATA
Primary IDE UDMA66/100	**Enabled** Disabled	Enables/disables UDMA 66/100 modes
Serial ATA	**Enabled** Disabled	Enables/disables SATA
SATA Controller Mode Option	Compatible **Enhanced**	Compatible: SATA/PATA devices are driven in legacy mode Enhanced mode: SATA/PATA devices are driven in native mode
AHCI Configuration	**Enabled** Disabled	Enables/disables the Advanced Host Controller Interface
Disable Vacant Ports	**Disabled** Enabled	Controls automatic disabling of vacant SATA ports
HD Audio device	Disabled **Auto**	Enables/disables the audio interface Auto: only enabled when present
AC97 Audio	Disabled **Auto**	Enables/disables AC97 Audio feature
AC97 Modem	**Disabled** Auto	Enables/disables AC97 Modem feature

Lan Options



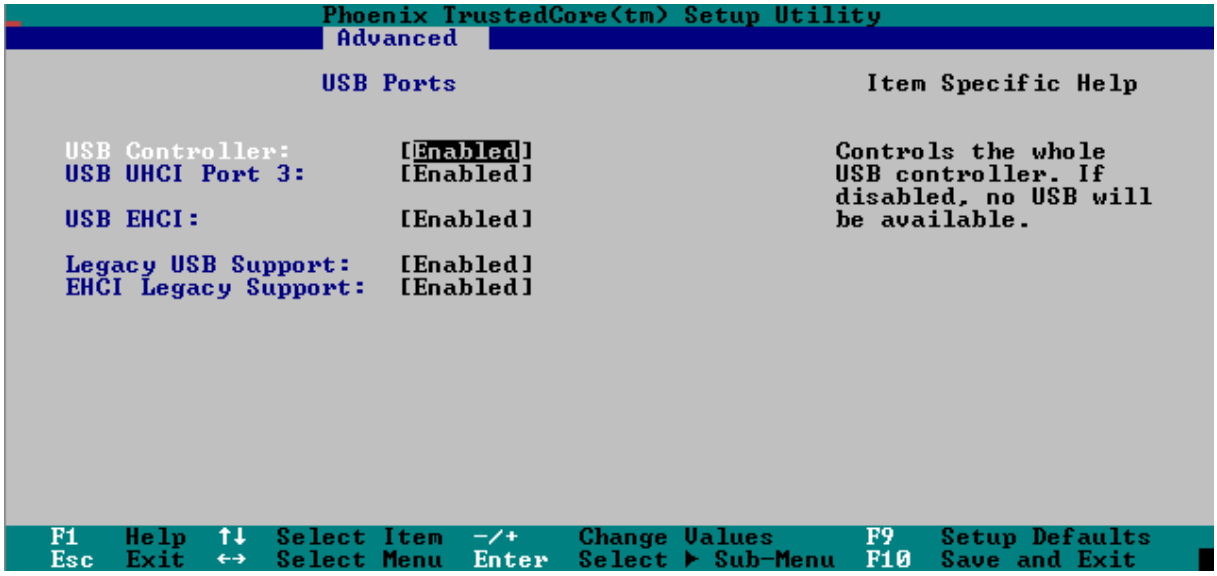
Feature	Option	Description
LAN Controller #1	**Enabled** Disabled	Enables/disables the PATA
Onboard LAN PXE ROM	Enabled **Disabled**	Enables/disables the LAN PXE boot ROM
Enable WOL	Enabled **Disabled**	Enables/disables Wake on LAN

Super I/O Controller Options



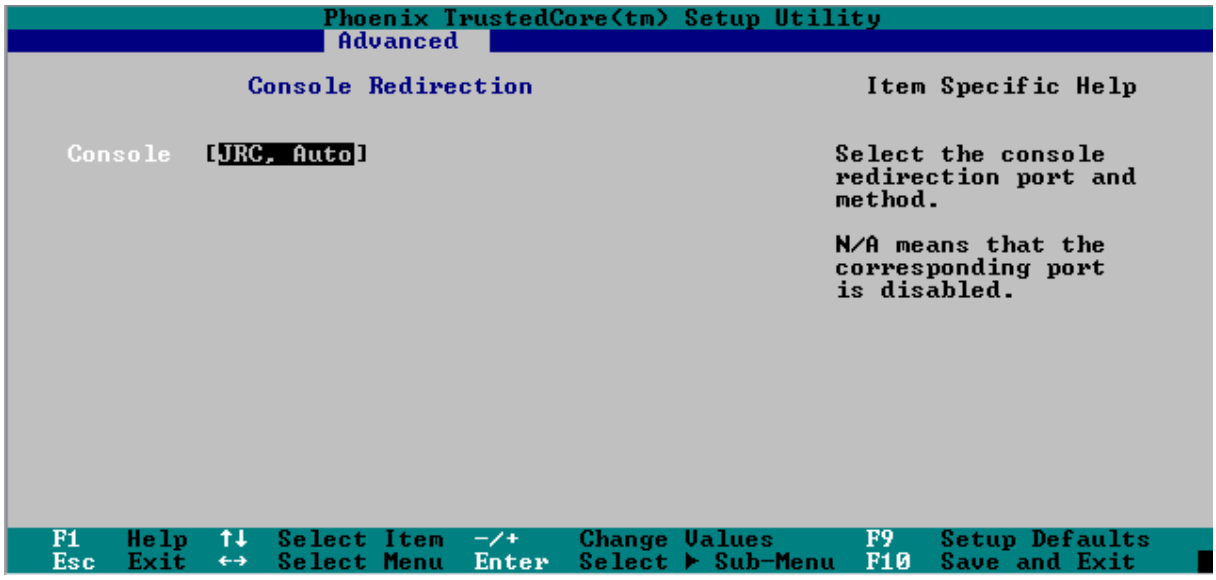
Feature	Option	Description
Onboard LPT	Auto Enabled **Disabled**	Enables/disables the Parallel Port
Serial Port A	**Enabled** Disabled Auto	Enables/disables serial port A; Auto: will be initialized when detected
Base I/O address	**3F8** 2F8	Base I/O address of COM port A
Interrupt	IRQ3 **IRQ4**	Selects interrupt of COM port A
Serial Port B	**Enabled** Disabled Auto	Enables/disables serial port A; Auto: will be initialized when detected
Mode	**Normal** IR ASK-IR	Sets the mode for COM port B
Base I/O address	3F8 **2F8**	Base I/O address of COM port B
Interrupt	**IRQ3** IRQ4	Selects interrupt of COM port B
External FDC	**Disabled** Auto	Enables/disables external Floppy Disk Controller
Serial Port C	**Disabled** Auto	Enables/disables external COM port C
Serial Port D	**Disabled** Auto	Enables/disables external COM port D
External LPT	**Disabled** Auto	Enables/disables external Parallel Port

USB ports



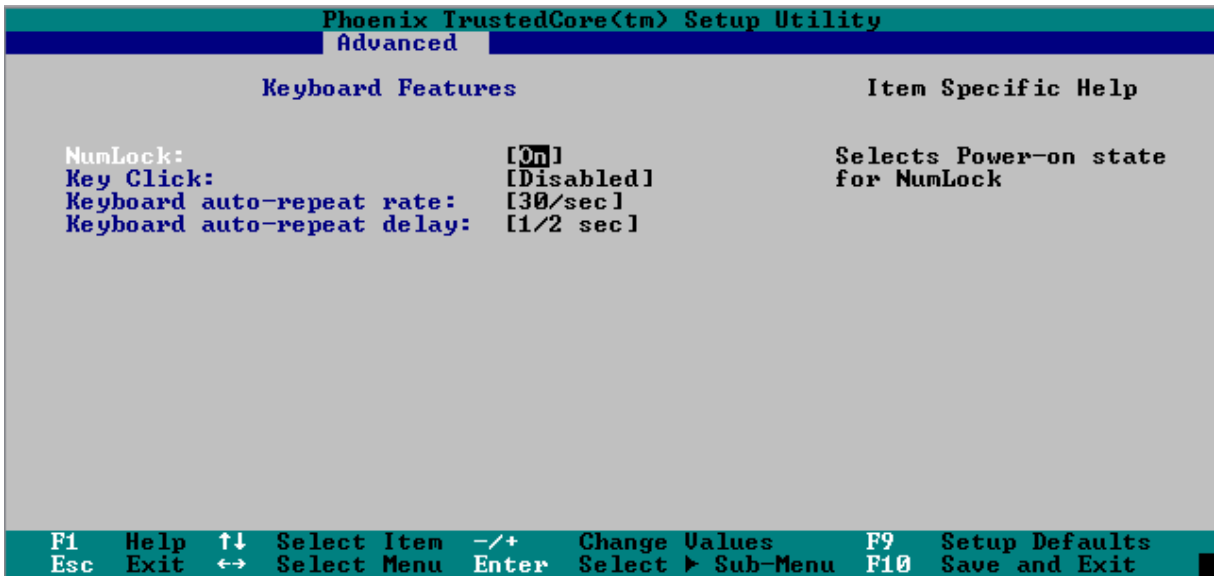
Feature	Option	Description
USB Controller	**Enabled** Disabled	Enables/disables the USB controller
USB UHCI Port 3	**Enabled** Disabled	Enables/disables USB Port 3 (USB line 5 and 6, which are not accessible)
USB EHCI	**Enabled** Disabled	Enables/disables USB 2.0 support
Legacy USB Support	**Enabled** Disabled	Enables/disables USB legacy support
EHCI Legacy Support	**Enabled** Disabled	Enables/disables USB legacy support in USB 2.0 mode

Console Redirection



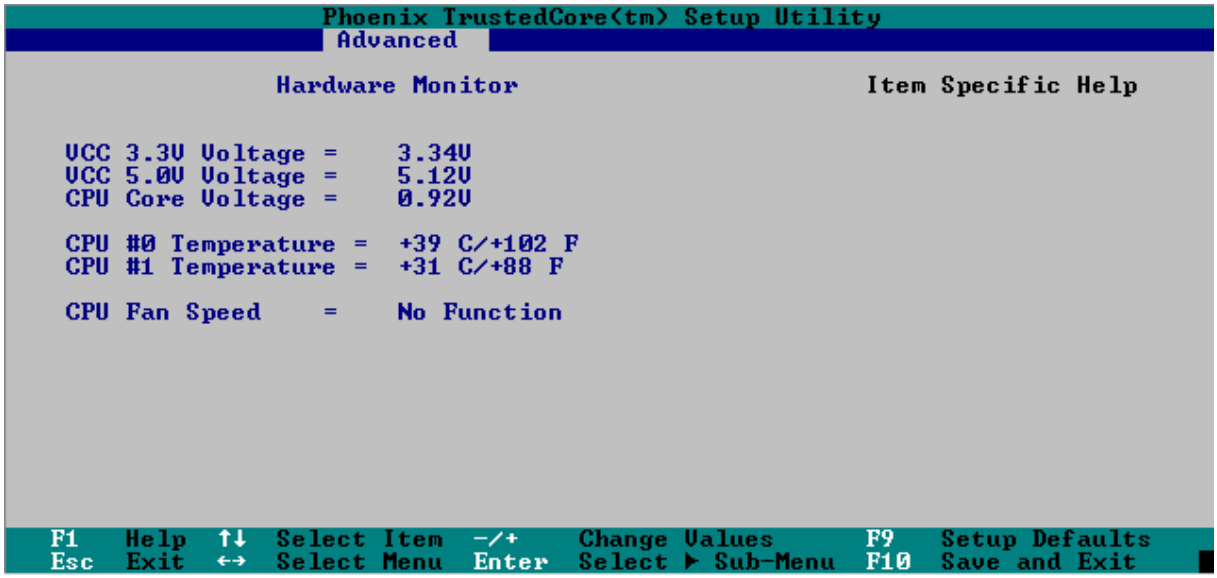
Feature	Option	Description
Console	Disabled UCR COM A UCR COM B UCR COM C UCR COM D **JRC, Auto**	Controls the serial console redirection. N/A

Keyboard Features Submenu

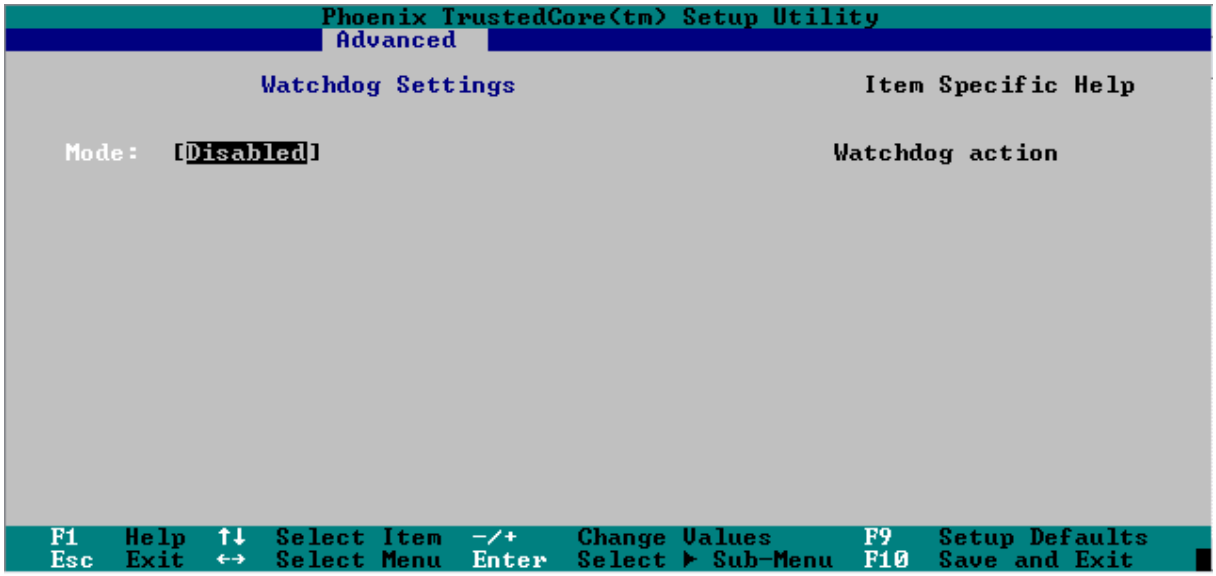


Feature	Option	Description
NumLock	Auto **On** Off	Selects Power-on state for NumLock
Key Click	**Disabled** Enabled	Enables Key Click
Keyboard auto-repeat rate	**30/sec** 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate
Keyboard auto-repeat delay	¼ sec **½ sec** ¾ sec 1 sec	Selects delay before key repeat

Hardware Monitor

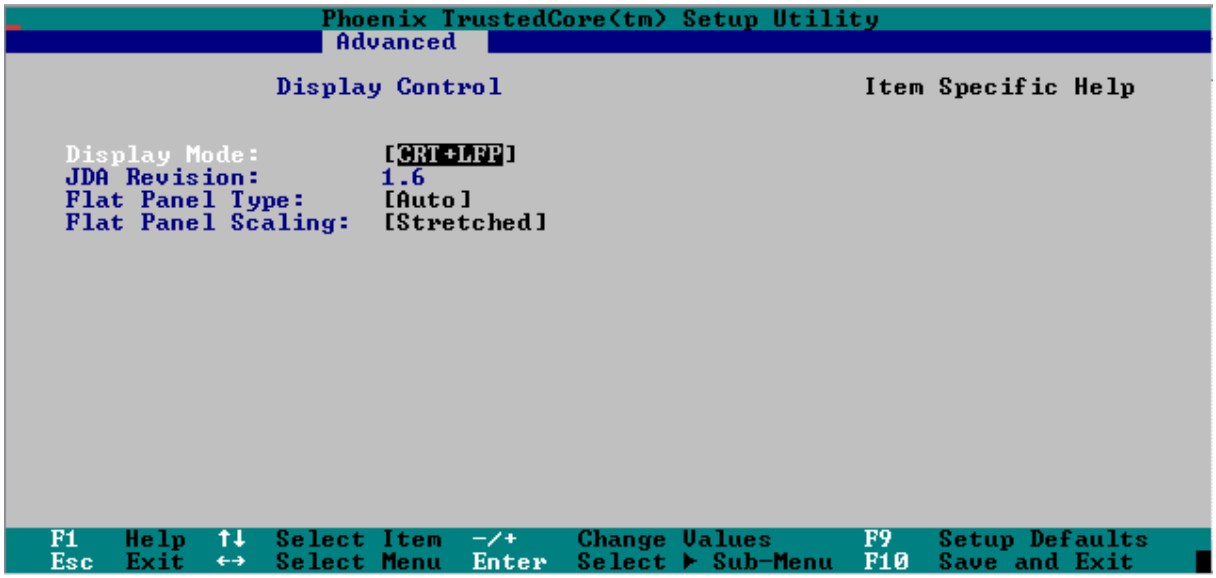


Watchdog Settings



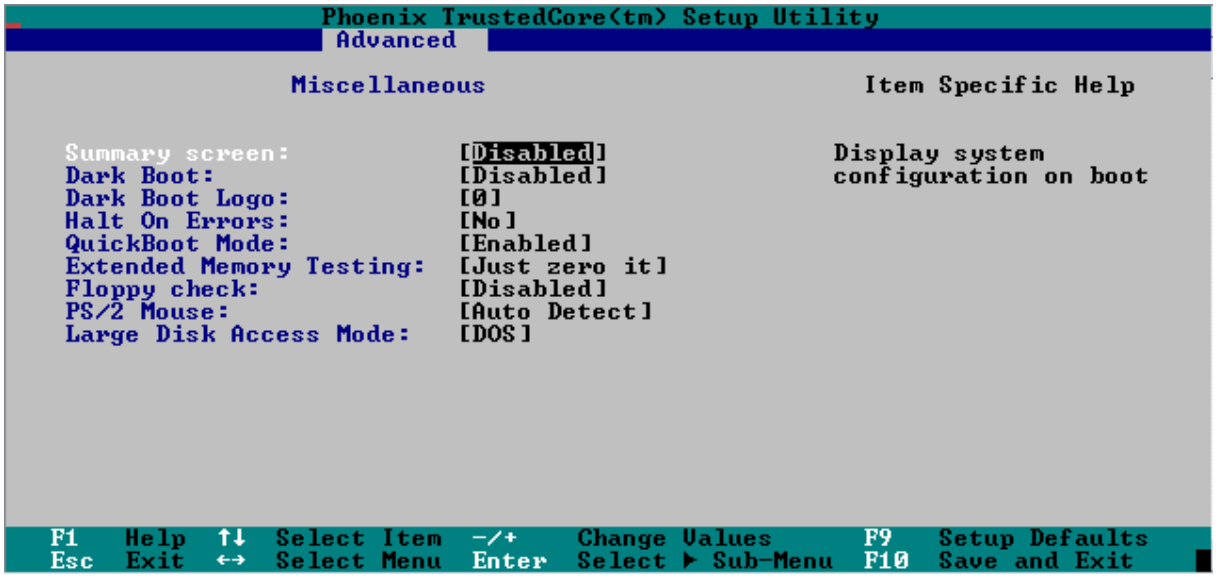
Feature	Option	Description
Mode	**Disabled** Reset NMI	Watchdog action
Timeout	1sec 5sec 10sec **30sec** 1min 5.5min 10.5min 30.5min	Max. trigger periode
Delay	1sec 5sec 10sec **30sec** 1min 5.5min 10.5min 30.5min	Time until watchdog timer starts to count

Display Control



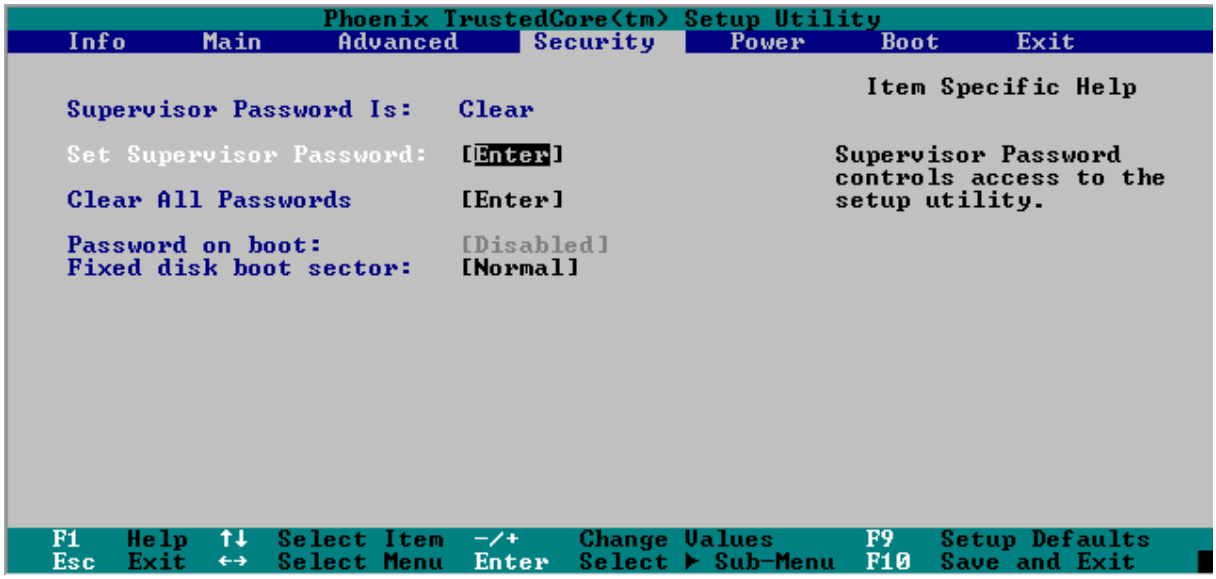
Feature	Option	Description
Display Mode	CRT only LFP only **CRT + LFP** LFP + EFP	CRT: Cathode Ray Tube LFP: LVDS flat panel (JILI) EFP: Embedded flat panel (sDVO)
Flat Panel Type	VGA 1x18 SVGA 1x18 XGA 1x18 XGA 1x24 SXGA 2x18 SXGA 2x24 UXGA 2x18 Enter PAID Enter FPID **Auto**	Select [Auto] for JILI or one of the predefined LCD's Use [Enter PAID] or [Enter FPID] to manually enter panel adapter ID or flat panel ID.
Flat Panel Scaling	Centered **Stretched**	

Miscellaneous Submenu



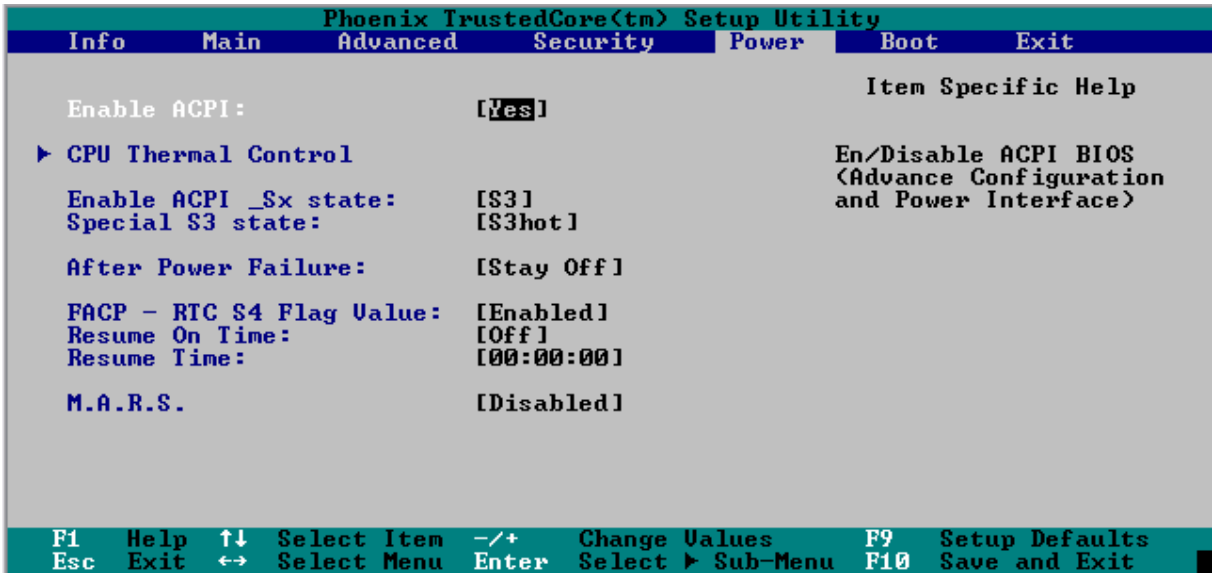
Feature	Option	Description
Summary Screen	**Disabled** Extended	Display system configuration at boot
Dark Boot	**Disabled** Enabled	Prevent diagnostic screen output during boot
Dark Boot Logo	**0** 1	Use -/+ to select the Dark Boot logo 0 – Vendor Logo 1 – Blank screen
Halt On Errors	**No** Yes	Determines if errors cause the system to halt
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Extended Memory Testing	Normal **Just zero it** None	Determines which type of tests will be performed on extended memory (above 1MB).
Floppy check	**Disabled** Enabled	Disables/Enables the floppy check during boot
PS/2 Mouse	Disabled Enabled **Autodetect**	Controls the usage of the PS/2 mouse
DMA channel	DMA 1 **DMA 3**	Set the DMA channel for the parallel port

10.3.4 Security Menu



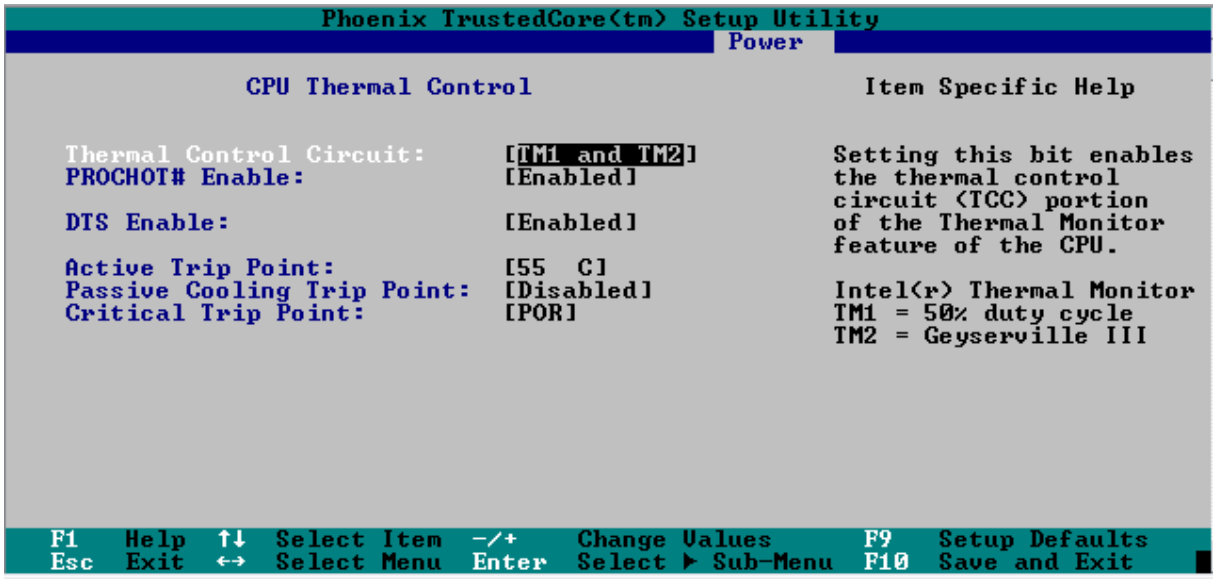
Feature	Option	Description
Set Supervisor Password	[a..z;0..9;+-#...]	Allows to set Supervisor Password
Clear All Passwords		Clear Supervisor and Administrative Password
Password on boot	**Disabled** Enabled	Enables/Disables password for boot process
Fixed Disk boot sector	**Normal** Write Protect	Enables/Disables Write protection of boot sector to protect against viruses

10.3.5 Power Menu



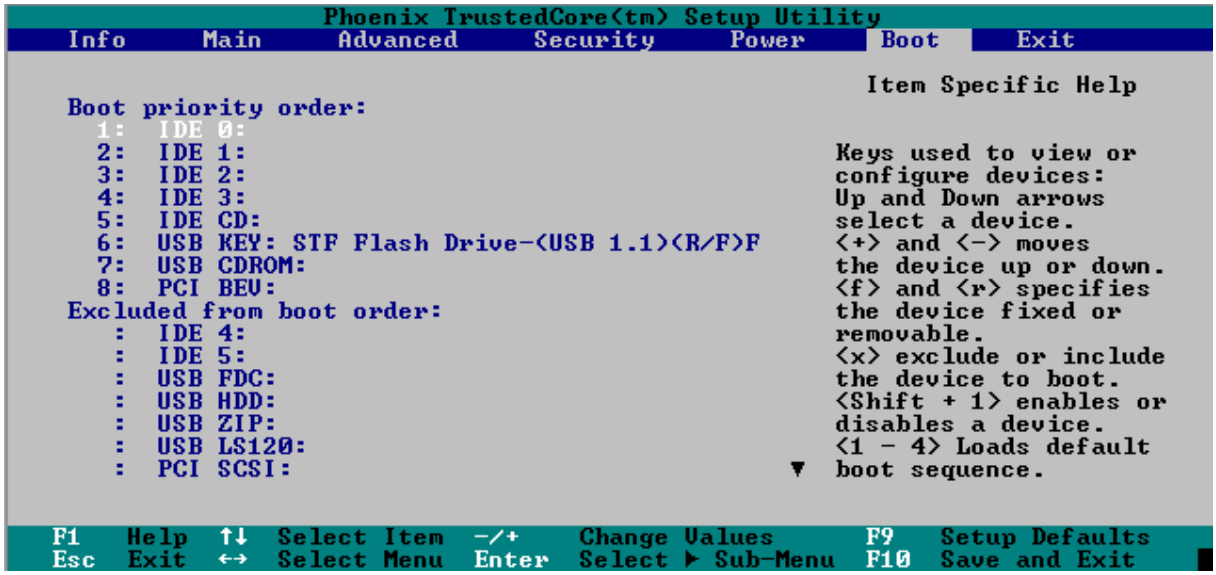
Feature	Option	Description
Enable ACPI	No **Yes**	En/Disable ACPI BIOS (Advance Configuration and Power Interface)
Enable ACPI _Sx state	None S1 **S3** S1+S3	This option allows to selectively enable Sx standby states for ACPI OS. Choosing 'None' will force the OS to have only S4 and S5 states.
Special S3 State	S3hot S3cold	Controlles if the 5V_Stb is switched off (S3cold) during S3 or stays on (S3hot)
After Power Failure	**Stay Off** Last State Power On	Sets the mode of operation if an AC/Power Loss occurs. The two modes are: Enabled restores the previous power state before loss occurred, Disabled keep the power off until the power button is pressed. The Disabled choice turns off Resume on Modem Ring.
FACP – RTC S4 Flag Value	Disabled **Enabled**	Valid only for ACPI. Control the value for the RTC S4 Flag in the FACP Table
Resume On Time	On **OFF**	Disables/Enables the Resume On Time Feature
Resume Time	[XX:XX:XX]	Sets the Time for the Rsume On Time Feature
M.A.R.S.	**Disabled** Enabled	Disables/Enables the support for the SMART battery control system M.A.R.S

CPU Thermal Control Circuit



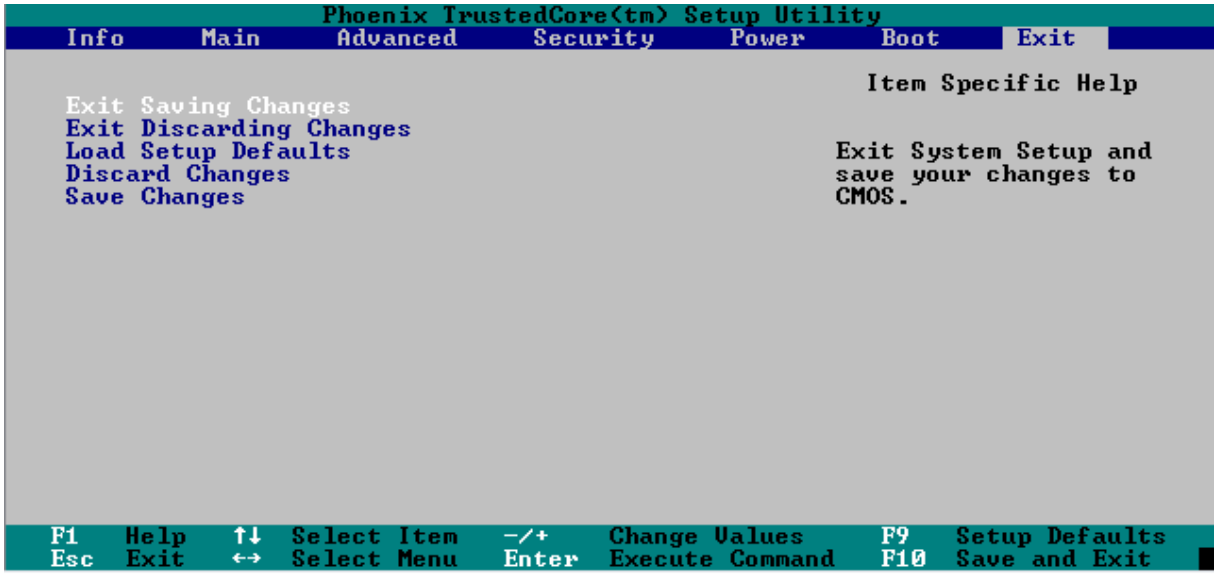
Feature	Option	Description
Thermal Control Circuit	Disabled TM1 TM2 **TM1 and TM2**	Sets the mode of the Thermal Control Circuit
PROCHOT# Enable	**Enabled** Disabled	This function engages the Thermal Control Circuit when enabled
DTS Enable	**Enabled** Disabled	Controls the DTS function of the processor
Active Trip Point	Disabled 15 C 23 C ... **55 C** 63 C ... 119 C	This value controls the temperature of the ACPI active trip point - the point in which the OS will turn on the CPU fan (connector on PCB). If DTS is enabled only values below 97°C are valid.
Passive Cooling Trip Point	**Disabled** 15 C 23 C ... 119 C	This value controls the temperature of the ACPI passive cooling trip point - the point in which the OS will start to throttle the CPU, either by TM1 or TM2. If DTS is enabled only values below 97°C are valid.
Critical Trip Point	**POR** 15 C 23 C ... 119 C 127 C	This value controls the temperature of the ACPI critical trip point - the point in which the OS will shut down the system. POR means 100°C for all Intel processors.

10.3.6 Boot Menu



Feature	Option	Descpription
Boot priority order	1:USB Key 2:USB CDROM 3:IDE CE 4:IDE 0 5:IDE 1 6:IDE 2 7:IDE 3 8:	Keys used to view or configure devices: Up and Down arrows select a device. <+> and <-> moves the device up or down. <f> and <r> specifies the device fixed or removable. <x> exclude or include the device to boot. <Shift + 1> enables or disables a device. <1 – 4> Loads default boot sequence.
Excluded from boot order	IDE 4 IDE5 USB FDC USB HDD USB ZIP USB LS120 PCI SCSI	

10.3.7 Exit Menu



Feature		Description
Exit Saving Changes		Exit System Setup and save your changes to CMOS.
Exit Discarding Changes		Exit utility without saving Setup data to CMOS.
Load Optimized Defaults		Load customer specific default values
Load Setup Defaults		Load default values for all SETUP items
Discard Changes		Load previous values from CMOS for all SETUP items
Save Changes		Save Setup Data to CMOS

10.4 Updating or Restoring BIOS

Phoenix Phlash16 allows you to update or restore the BIOS with a newer version or restore a corrupt BIOS by using a floppy disk without having to install a new ROM chip.

➤ Get the Phoenix Phlash16 compressed file, CRDxMODB.ZIP, from the Kontron Embedded Modules GmbH. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the Flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISES.EXE.
BIOS.WHP	Serves as the actual BIOS image to be programmed into Flash ROM.

➤ BIOS.WPH is a file that contains the 1MB BIOS binary and flash interface code required by Phlash16.EXE.

➤ To install Phoenix Phlash16 on a hard disk, unzip the content of CRDxMCAL.ZIP into a local directory such as C:\PHLASH.

Note: Crisis Recovery requires either a floppy disk connected to the LPT interface (external floppy drive_1) or an USB floppy drive.

➤ To create a Crisis Recovery Diskette, insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the Flash ROM.
BIOS.WPH	Serves as the BIOS image to be programmed into Flash ROM.

➤ If the BIOS image (BIOS.WPH) changes because of an update or bug fix, copy the new BIOS.WPH image onto the diskette.

➤ Phoenix Phlash16 runs in one of two modes: Command Line or Crisis Recovery. Use the Command Line mode to update or replace a BIOS. To execute Phlash16 in this mode, move to the Crisis Recovery Disk and type PHLASH16. Phoenix Phlash16 will update the BIOS. Phlash16 can fail if the system uses memory managers. If this occurs, the utility displays the following message:

Cannot flash when memory managers are present.

➤ If you see this message after you execute Phlash16, disable the memory manager or use parameter /x for Phlash16.exe.

10.5 Preventing Problems When Updating or Restoring BIOS

Updating the BIOS represents a potential hazard. Power failures or fluctuations that may occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.
To prevent this potential hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above). Additionally, the end user can insert an update key into the serial port (COM1 only) to force initiating the recovery routine for the boot block.

11 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL□0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

11.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1.

  The name of the first device installed will be returned.

  If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL□0).

  You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Embedded Modules GmbH Web site, for further information on implementing and using JIDA calls with C sample code.

12 Appendix B: PC Architecture Information

The following sources of information can help you better understand PC architecture.

12.1 Buses

12.1.1 ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

12.1.2 PCI/104

- Embedded PC 104 Consortium
- The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

12.1.3 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

12.2 Ports

12.2.1 RS-232 Serial

- EIA-232-E standard
- The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor

  The Interface Data Book includes application notes. Type “232” as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

12.2.2 Serial ATA

- Serial AT Attachment (ATA) Working Group. This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

12.2.3 USB

- USB Specification.
- USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

12.2.4 Programming

- C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer’s Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

- The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

13 Appendix C: Document Revision

Rev.	Date	Author	Changes
0.3	17.04.07	UMA	Created preliminary manual.
1.0	05.03.08	UMA	Added power measurements, added BIOS setup notes, fixed small issues, added note at height specification, added chapter "Limitations"